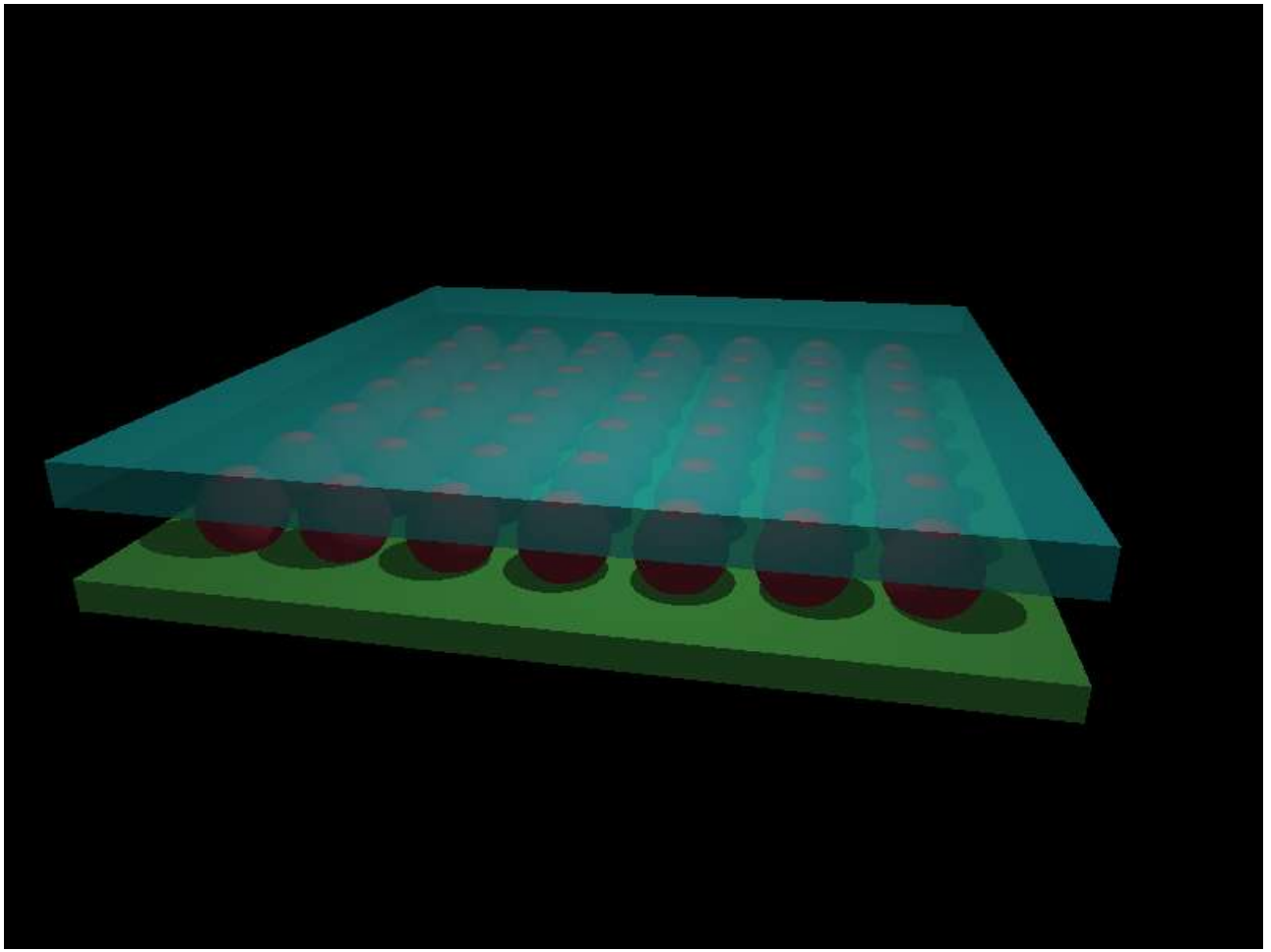
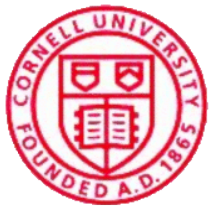
Pixel Array Detector for Single Particle Scattering



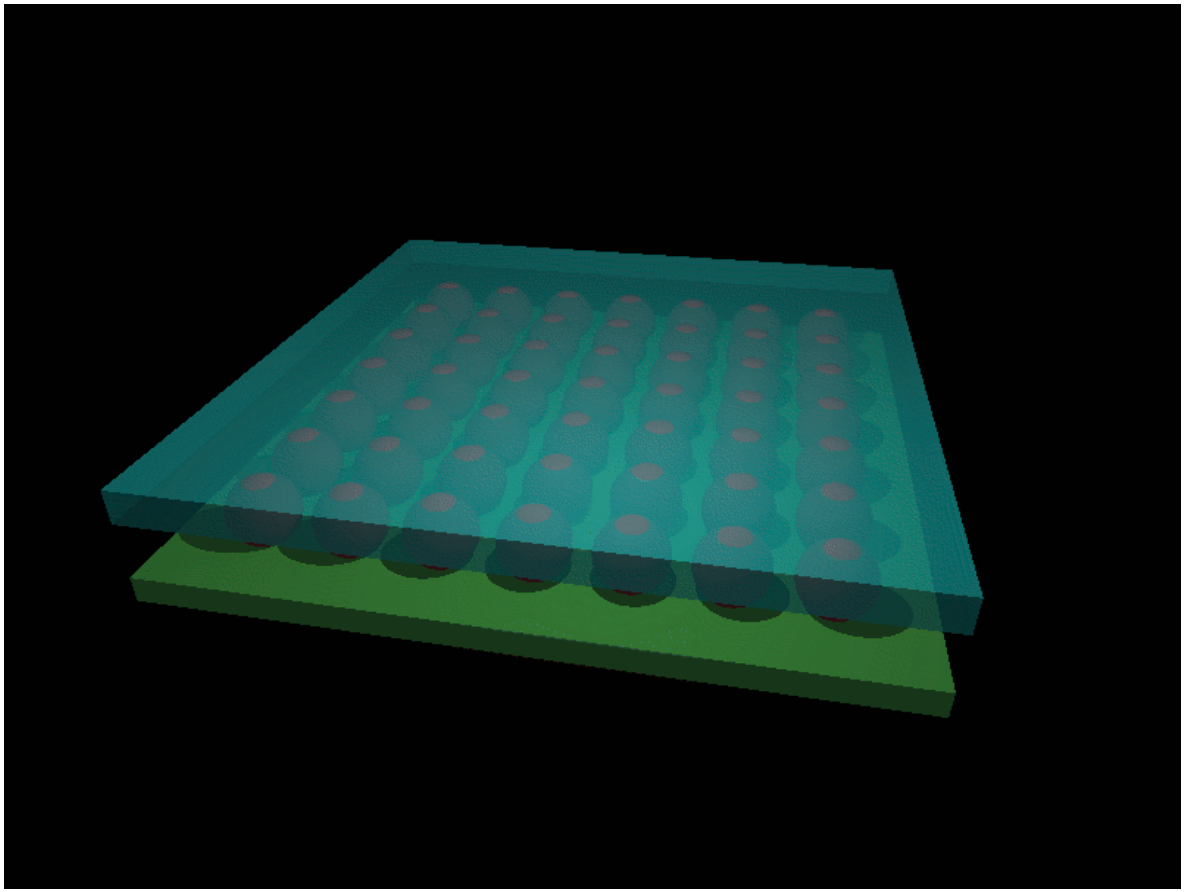


Outline

- Pixel Array Detectors: General Background.
  - Basic structure, diode, ASIC, bump-bonding.
- Specific requirements for LCLS PAD detector.
  - Noise, frame rate, efficiency, RAD hardness.
- Approach used in the first prototype.
  - front-end and pixel architecture.
- Test results from first prototype.
- Plans for next submission (second prototype).
- Conclusions and future.

Pixel Array Detectors

- Basic structure

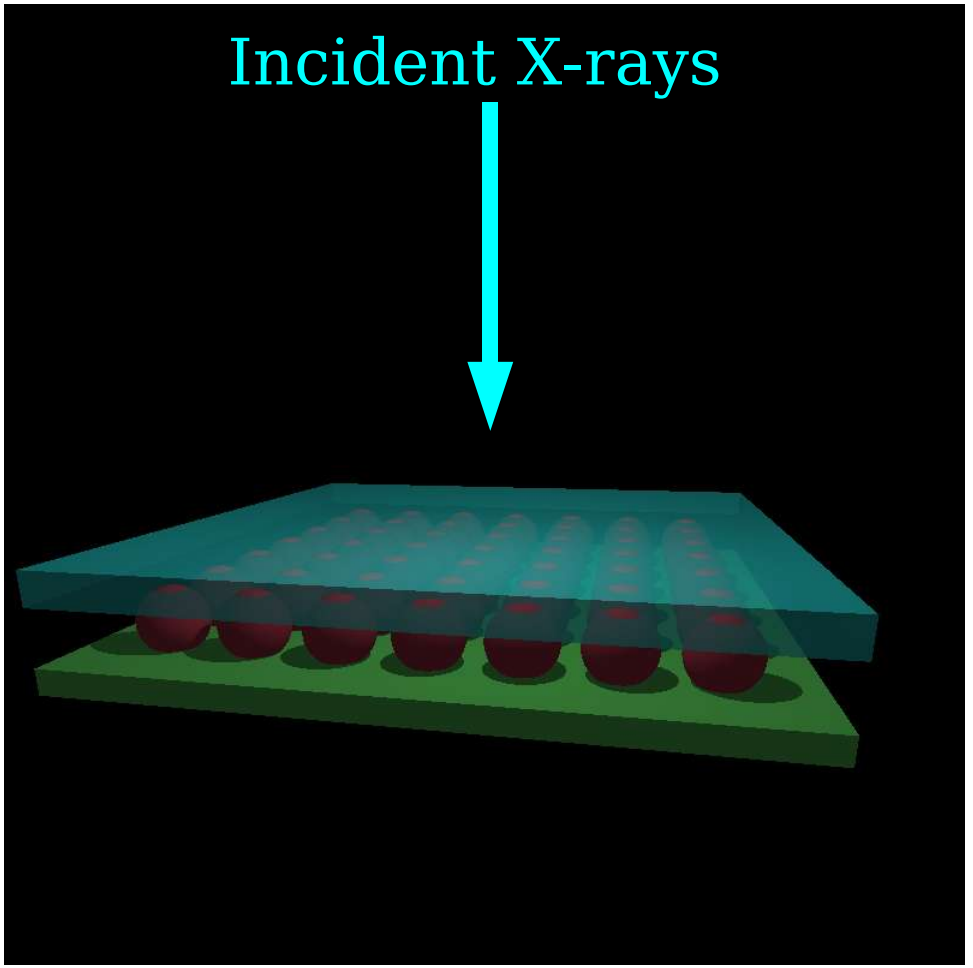


- High resistivity Si diode for direct x-ray conversion.

- Solder or indium bump-bonding connection to CMOS ASIC.

- CMOS ASIC uses high-quality commercial mixed-mode process 0.25 µm process.

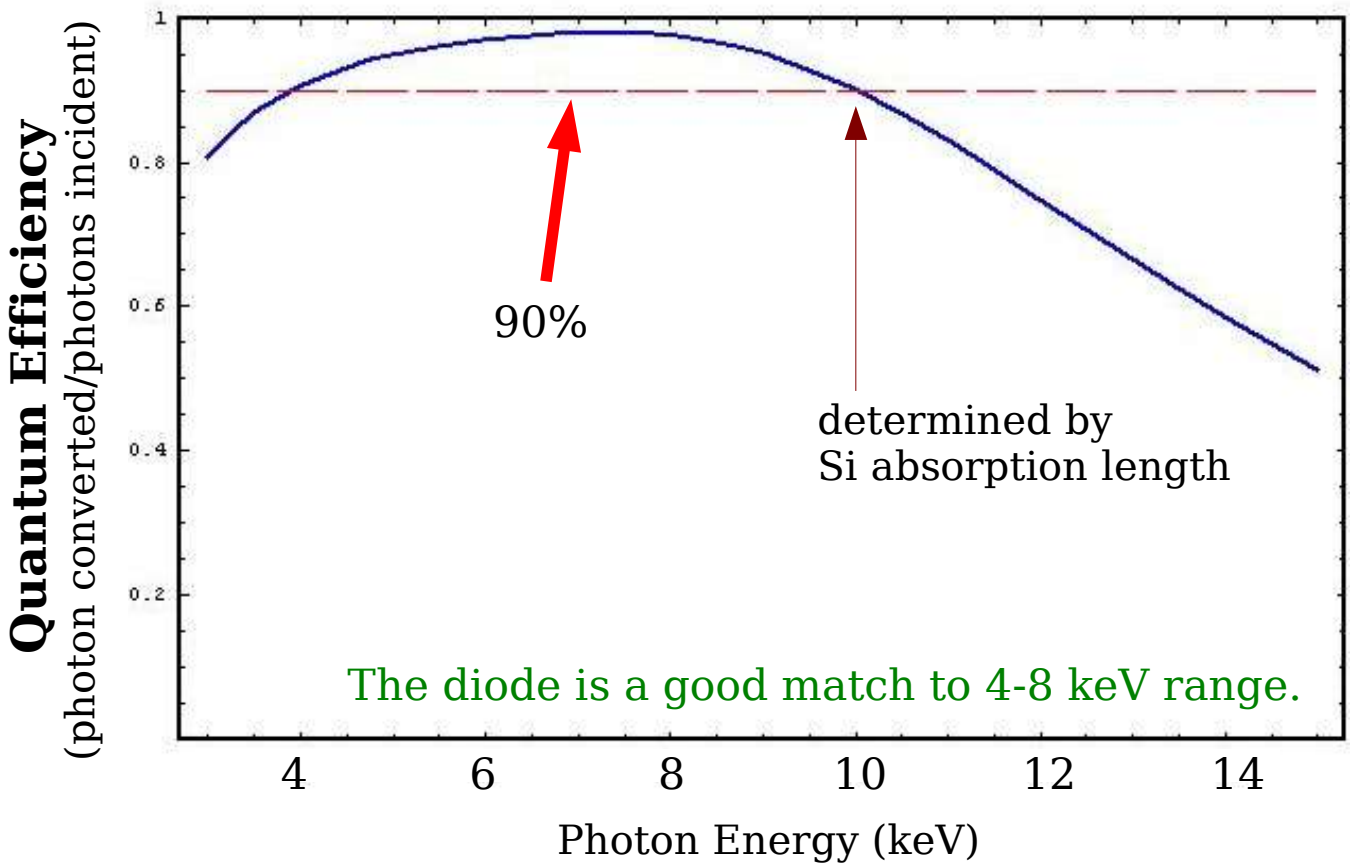
Detector Diode - Basics

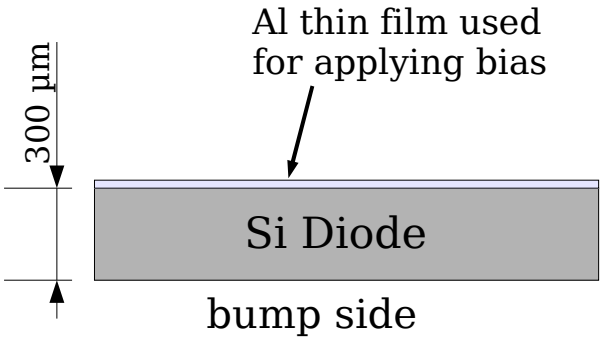


- Diode: direct conversion of x-rays.
- 300 μm thick silicon.
- Reverse biased for full depletion.
- ~2200 e-/hole pairs per 8 keV x-ray.
- Conversion noise dictated by Fano factor.

Diode Efficiency

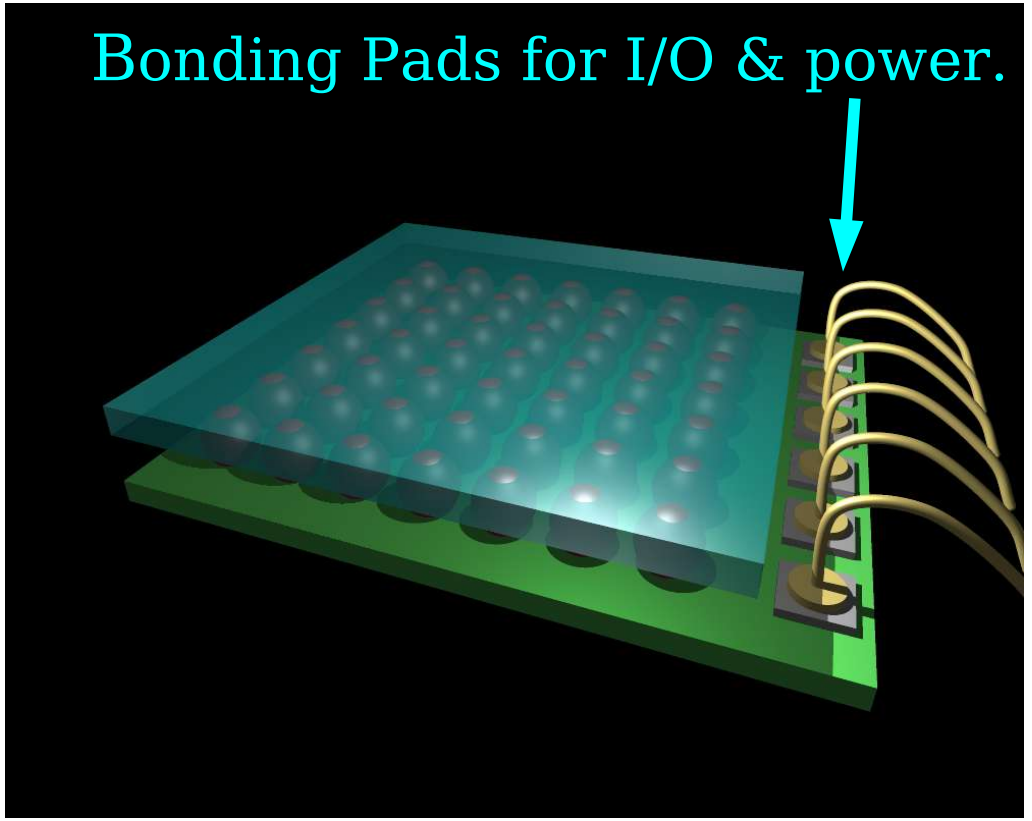
- Calculated quantum efficiency of diode detector using conservative assumptions.





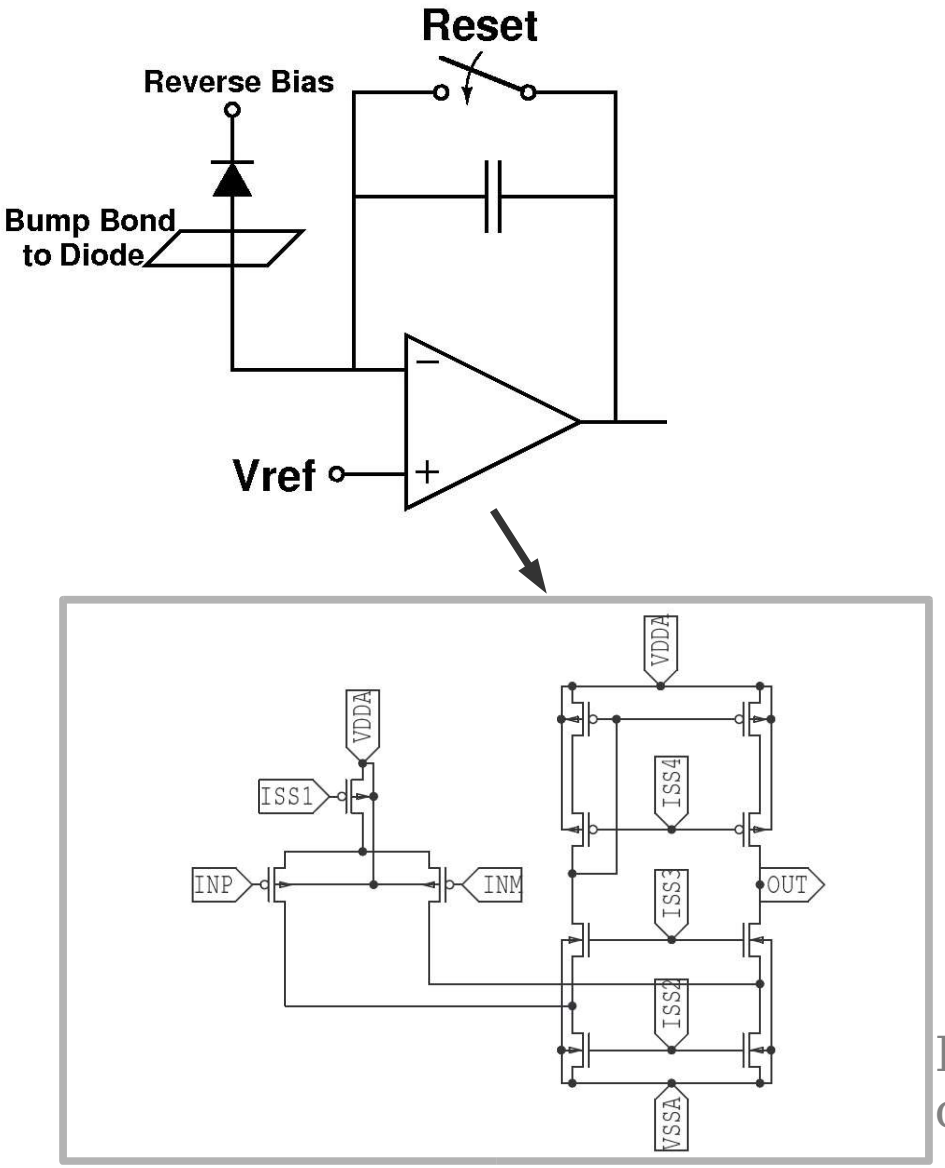
Values calculated for x-rays with normal incidence.

ASIC basics



- CMOS based.
- Pixels between 100 and 200 µm square in previous detectors.
- Commercial Process (TSMC 0.25 µm).
- Limit on size: 21mm square – single FOV.
- Top side PAD connections for I/O, power, and bumping to diode.
- 3-side buttable.

ASIC – pixel front-end



- Analog PAD's integrate charge.
- Charge is well defined per unit x-ray.
- Good at handling split events between pixel.
- AND – Needed for high flux measurements!!

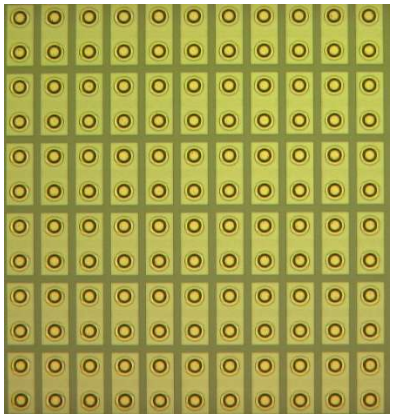
(i.e. when photons come faster than you can count!)

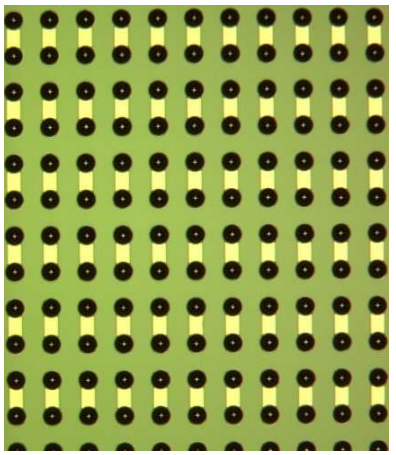
First LCLS-prototype single-stage folded cascode front-end op-amp.

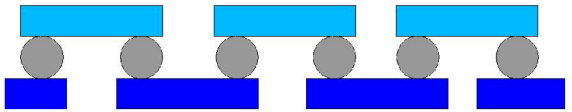
ASIC
Mixed Mode

- Mixed mode CMOS process
  - TSMC 0.25 µm process used in mobile phones.
- Allows monolithic combination of analog and digital circuits.
  - essentially by including high-quality metal-oxide-metal capacitors in the process.
- Some inherent radiation hardness.

Bump-bonding



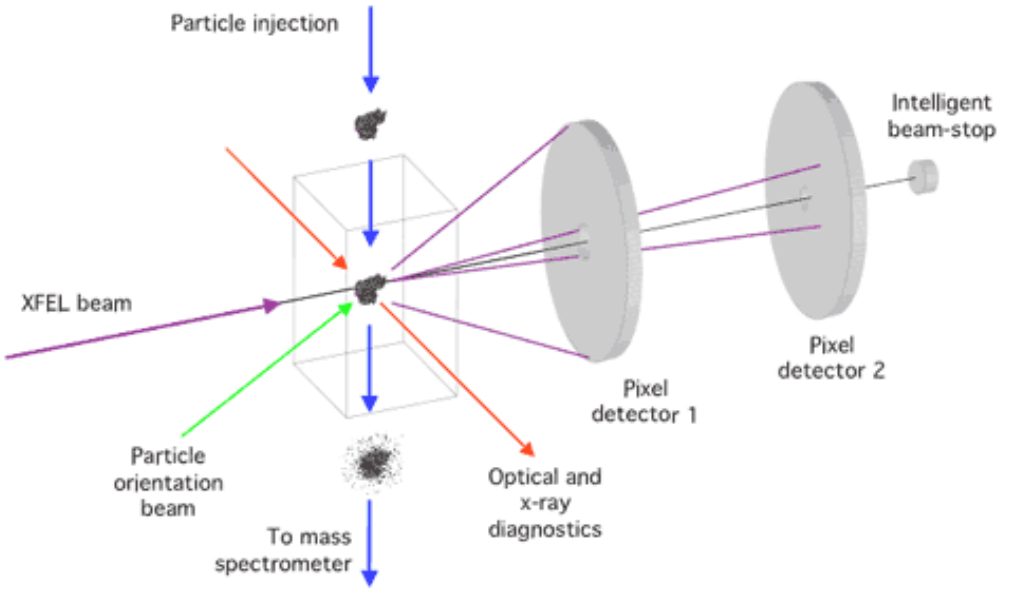




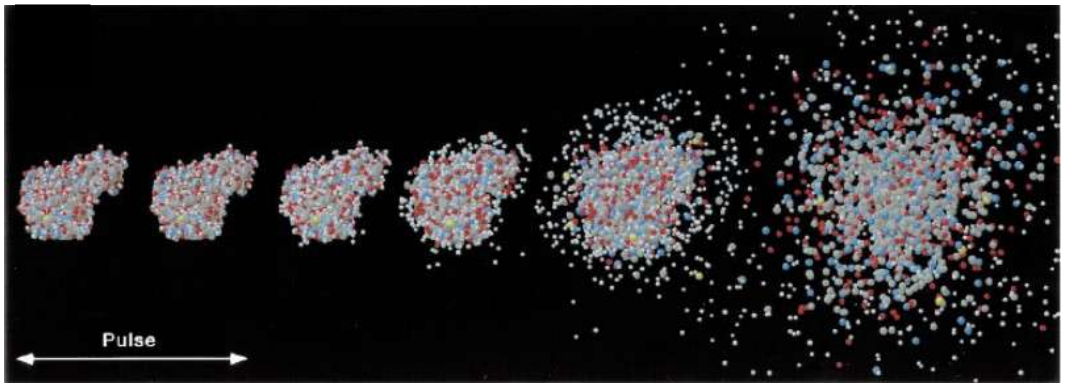
Above: Bumping test structures.

- Typically solder or indium bumping.
- Critical step for the detector.
- There are standard processes used in industry.
- Difficult for small volume research to do it for reasonable cost.

Single Particle Scattering



- Intense femtosecond pulses.
- 120 Hz frame rate.
- Single photon sensitivity.



LCLS Detector Requirements

Parameter	Requirement
Energy Range	4-8 keV
Well-depth/pixel	10^3
Readout frame rate	120 Hz
Signal/Noise	>3 for single 8 keV photon
DQE	> 90% at 8 keV
Pixel size	100-200 μm
Detector area	> 500x500 pixels

The question:

- Given these specs, how do we get the performance we want in a PAD?

- Some are addressed by the diode: DQE, Energy range.
- 500x500 means tiling is necessary.

LCLS Detector Requirements

Parameter	Requirement
Energy Range	4-8 keV → diode
Well-depth/pixel	10^3 → set by int. cap.*
Readout frame rate	120 Hz
Signal/Noise	>3 for single 8 keV photon
DQE	> 90% at 8 keV
Pixel size	100-200 μm → enough for electronics to fit in.
Detector area	> 500x500 pixels → Requires tiling

*$$C = \frac{dQ}{dV} = \frac{N_p(2200\frac{e-}{photon})(1.602\,10^{-19})}{2.2\,V} \approx 160\,fF$$

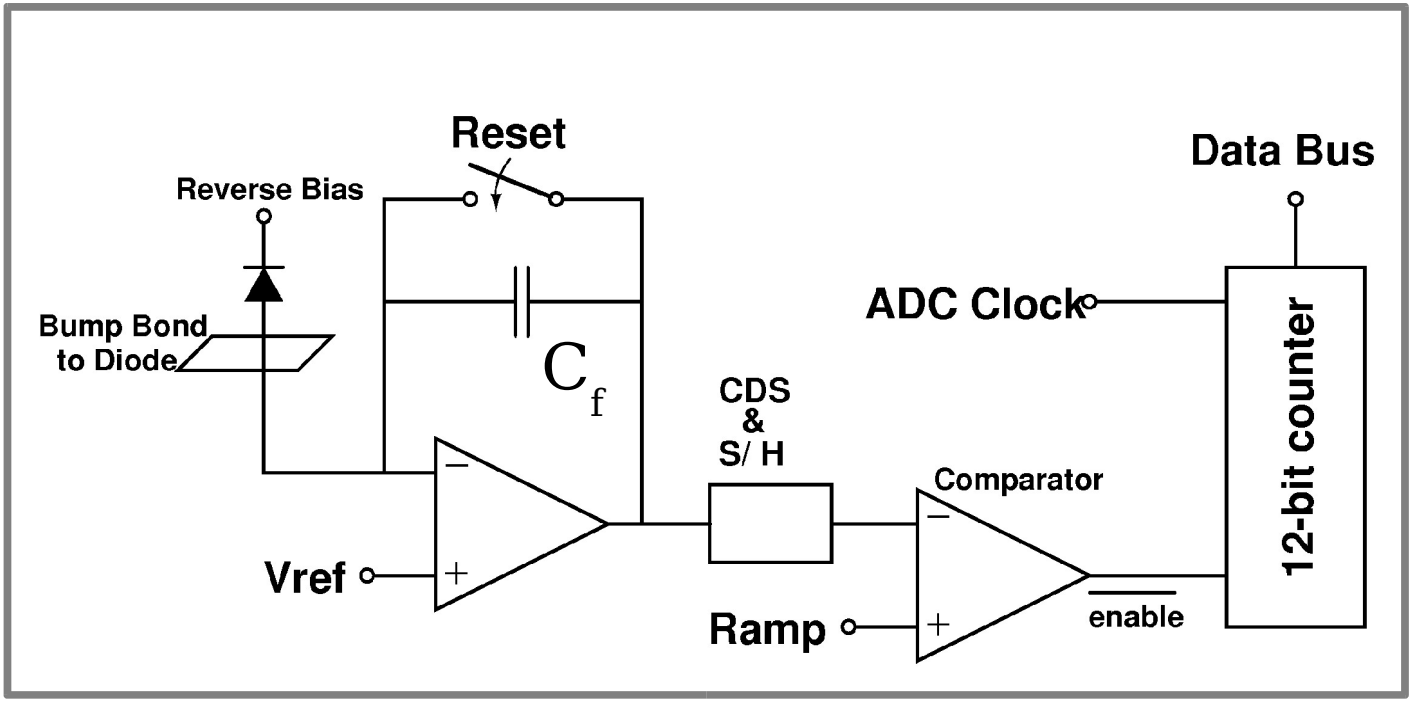
for N_p = number of photons = 1000

The question:

- Given these specs, how do we get the performance we want in a PAD?

- Some are addressed by the diode: DQE, Energy range.
- 500x500 means tiling is necessary.

High-level layout of LCLS pixel

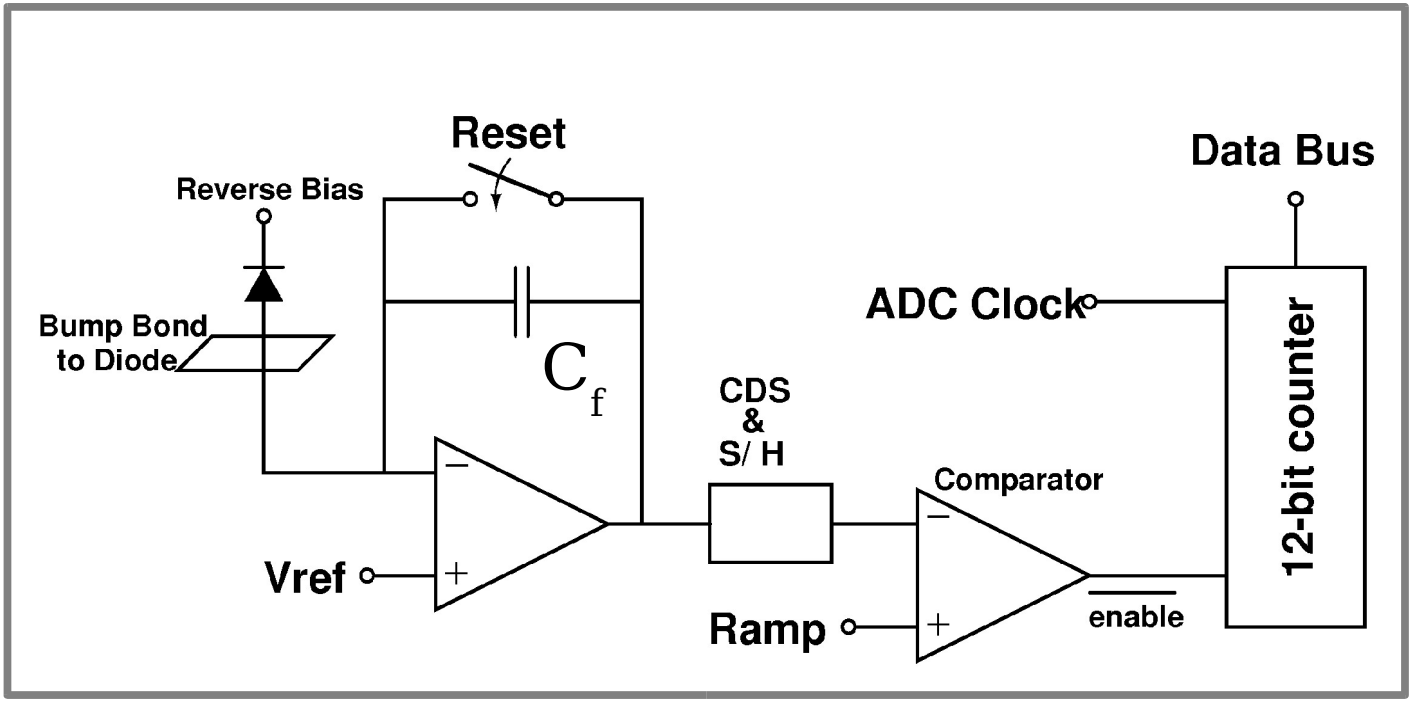


Simplified High-level view of proposed pixel

- In-pixel digitization using single-slope ramp (externally supplied).
- Each pixel converts independently and in parallel.
- Eliminates fast analog multiplexing.

Pixel similar to that in: S. Kleinfelder, S. Lim, X. Liu, and A. Gamal, "A 10000 Frames/s CMOS Digital Pixel Sensor", IEEE J. of Solid-State Circuits, vol. 36, no. 12, Dec. 2001.

High-level layout of LCLS pixel

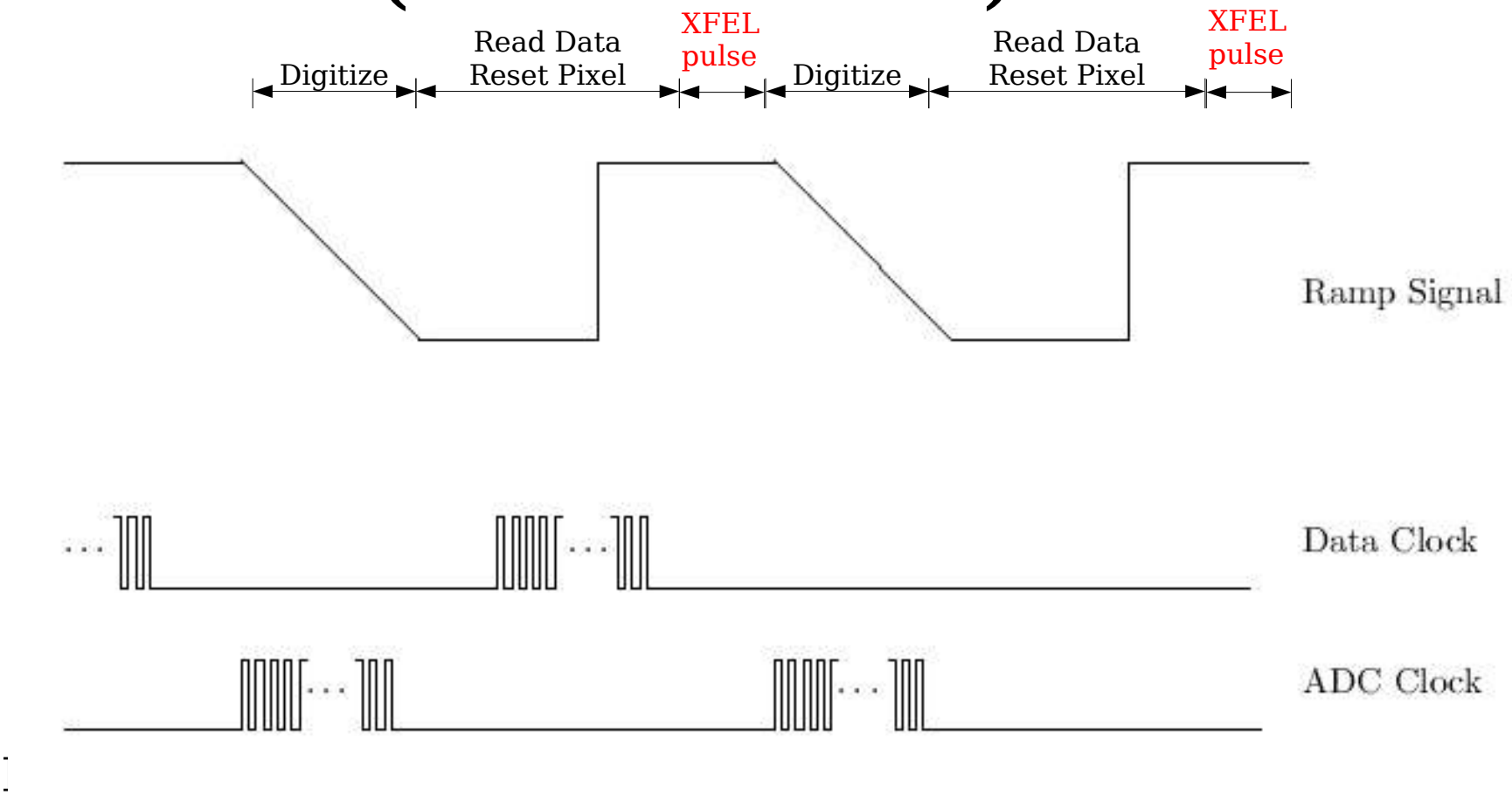


Simplified High-level view of proposed pixel

- Makes slow, low-bandwidth ADC possible.
- Only digital output.
- Keeps pixel level electronics simple.
- Easily adjustable input ramp.
- 120 Hz frame rate.

Pixel similar to that in: S. Kleinfelder, S. Lim, X. Liu, and A. Gamal, "A 10000 Frames/s CMOS Digital Pixel Sensor", IEEE J. of Solid-State Circuits, vol. 36, no. 12, Dec. 2001.

Digitization Scheme (waveforms)

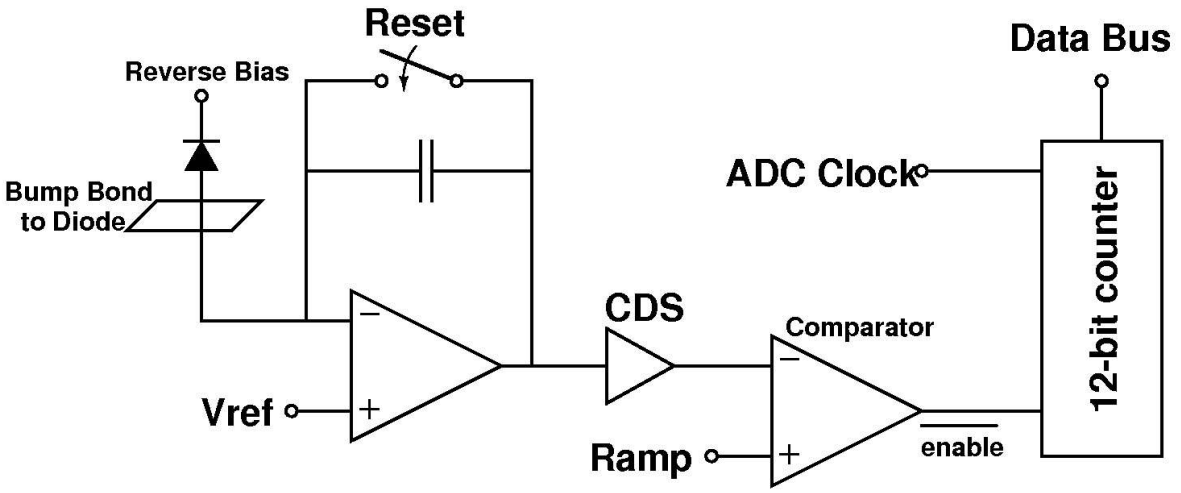


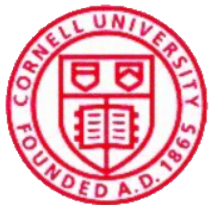
Basic idea: Take on the order of ms to digitize, then read out the data as fast as you can.

Pixel Design

general comments

- In-pixel single-slope ramp ADC.
- CDS stage has low bandwidth buffer.
- Latched output on the comparator.
- Relatively slow comparator.
- 12-bit counter/ shift-register.
- Parallel conversion of pixels.
- Programmable multiple-gain techniques available.





Digital Feedthrough Isolation

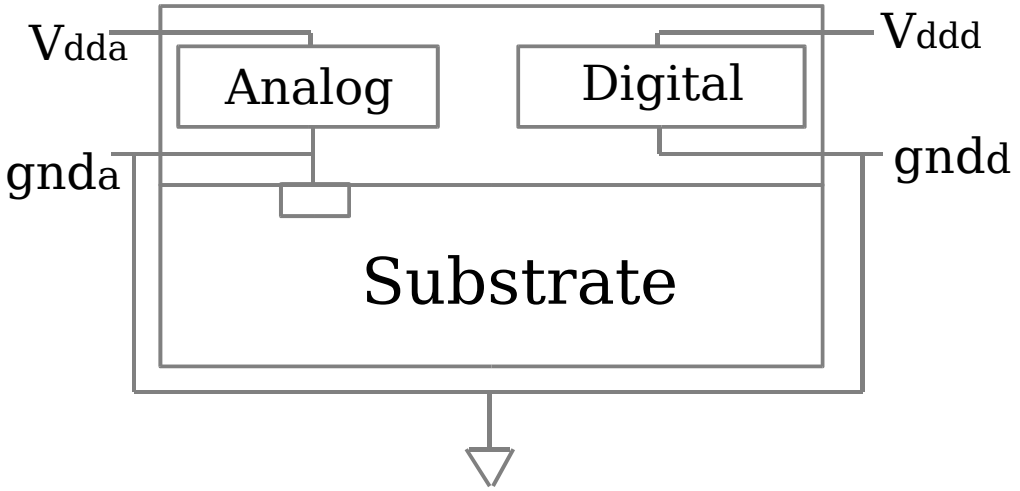
and more comments on approach

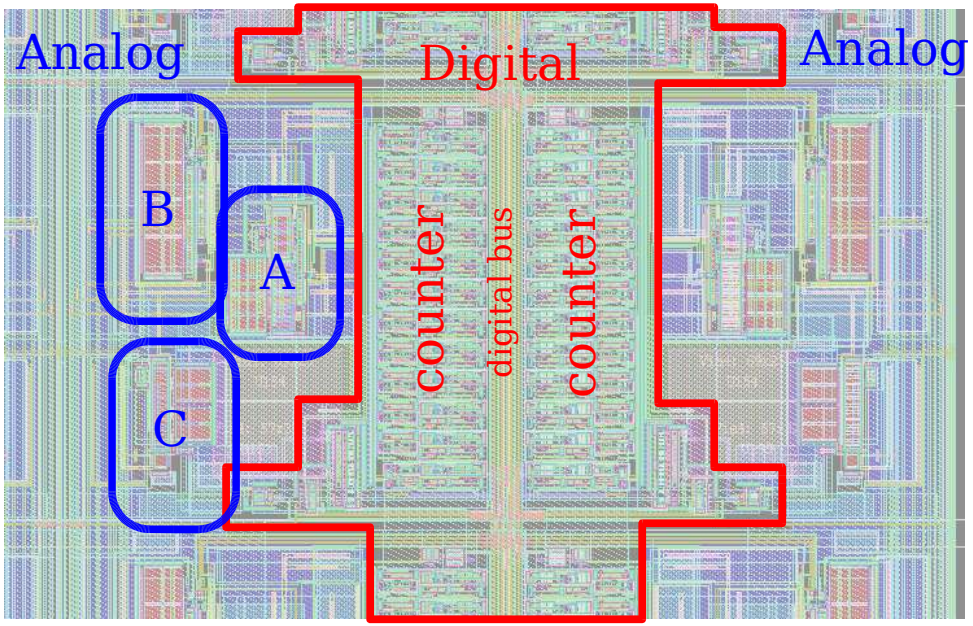
- Noise injection to analog front-end from digital clock.

What we are doing to reduce this:

- Full separation of anlog and digital power on chip.
- Low bandwidth buffer input to comparator.
- Highly shielded ramp signal.
- Slow comparator.
- Latched comparator output.

Power Layout





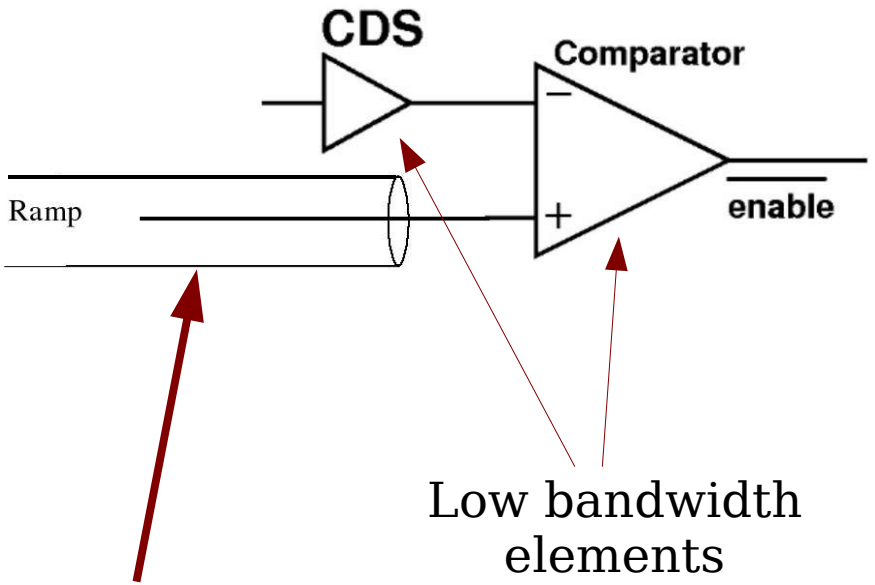
- Digital and power separated on chip.
- No DC connections between analog and digital power on chip.
- Still AC coupling through substrate.

A: Front End Amp.
B: CDS Buffer.
C: Comparator.

digital/analog division in adjacent mirrored pixels (LCLS proto-1)

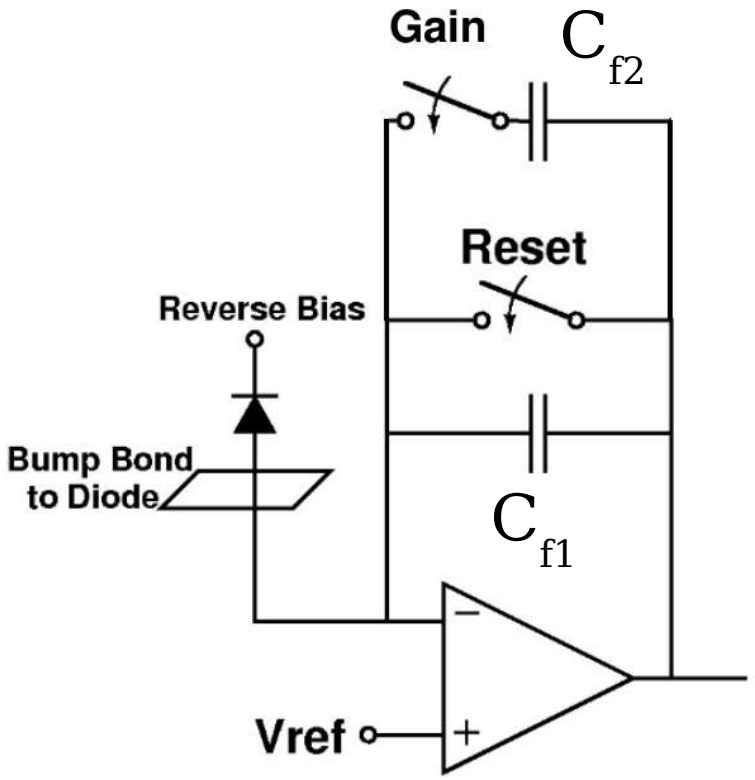
Buffer, Comparator and Ramp

(the heart of the ADC)



- Low bandwidth elements:
  - Buffer: ~1 Mhz (unity gain bw)
  - Comparator: < 1 MHz
- Heavily shielded ramp:
  - dedicated shield pads.
  - versatile waveform.

Well Depth and Multiple Gain



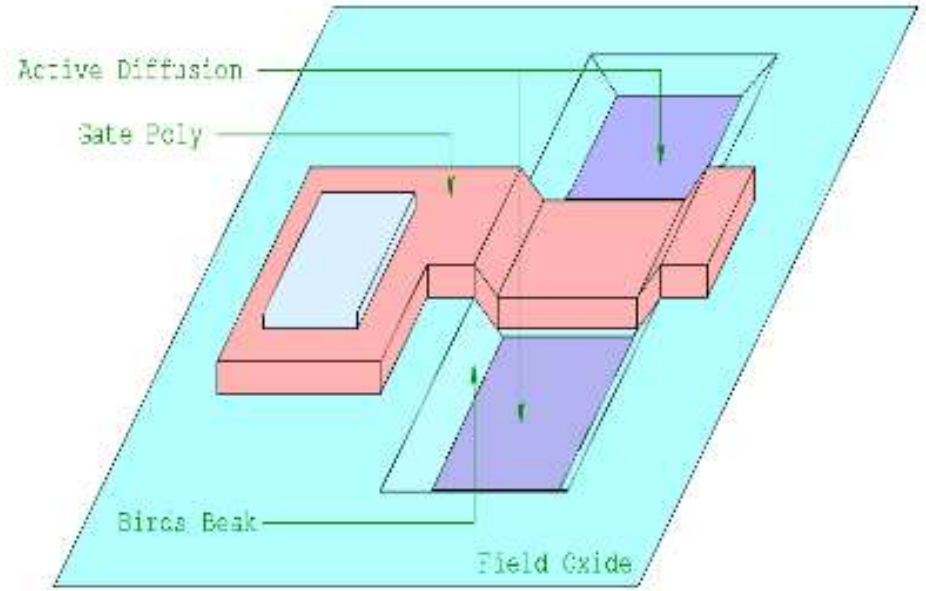
- In-pixel memory to set gain bit.
- C_{f1} – e.g. 50fF.
  - High gain full-well.

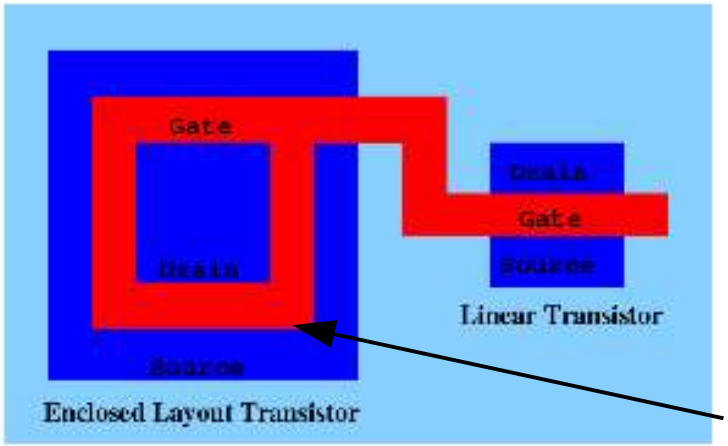
    300 x-rays

    7mV/x-ray.
- C_{f2} – e.g. 350 fF
  - low gain full-well

    2.5k x-rays.

Radiation Hardness





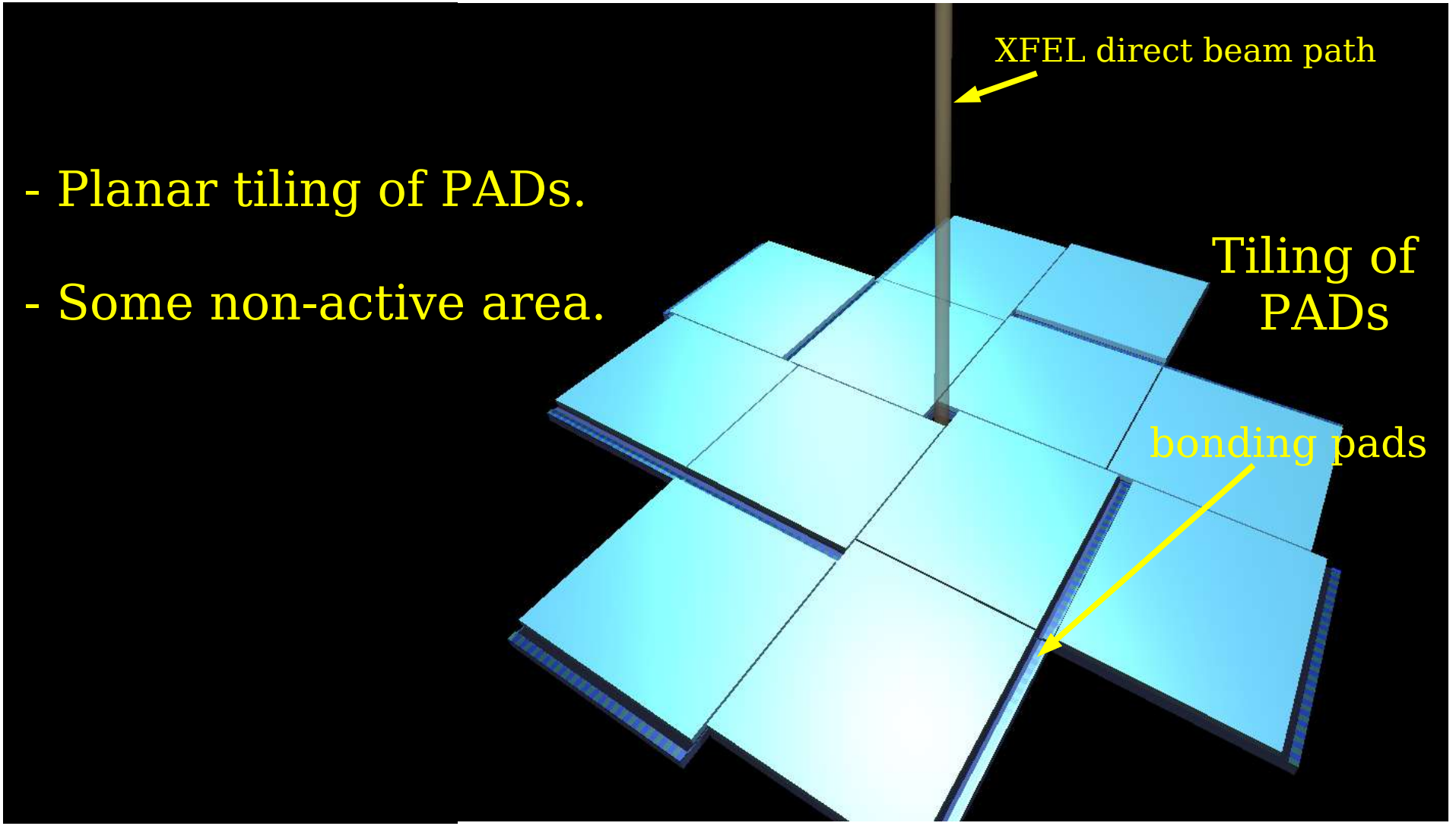
- Two major CMOS effects:
  - leakage currents in NMOS switches.
  - Threshold voltage shifts.
- Thinner oxides in 0.25 μm help.
- Diode damage
  - leakage not a problem with short exposures.

Enclosed Layout Transistor

Tiling

- Planar tiling of PADs.

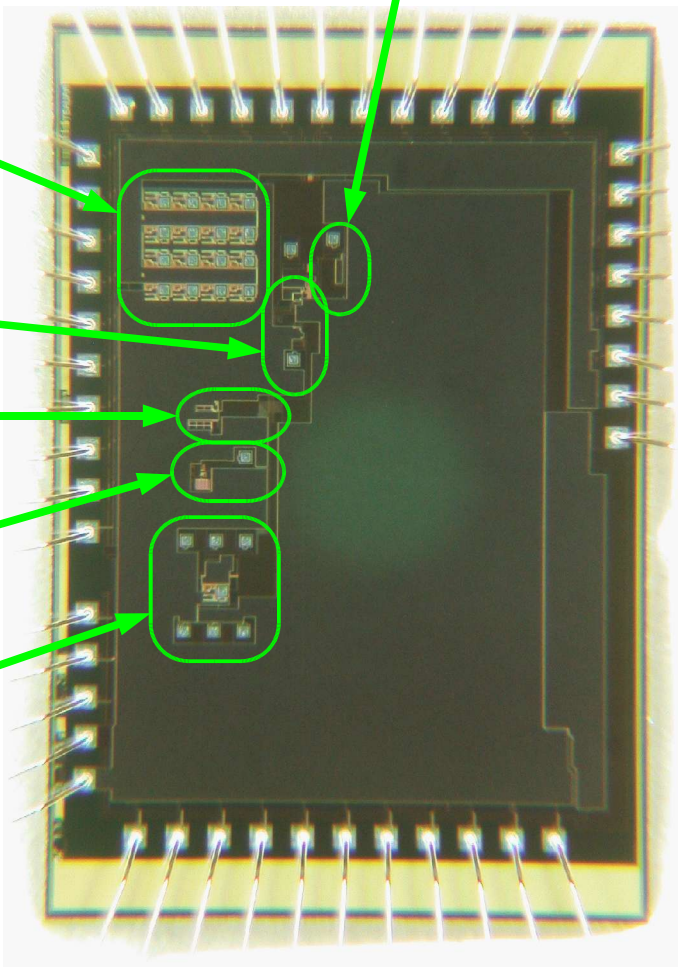
- Some non-active area.



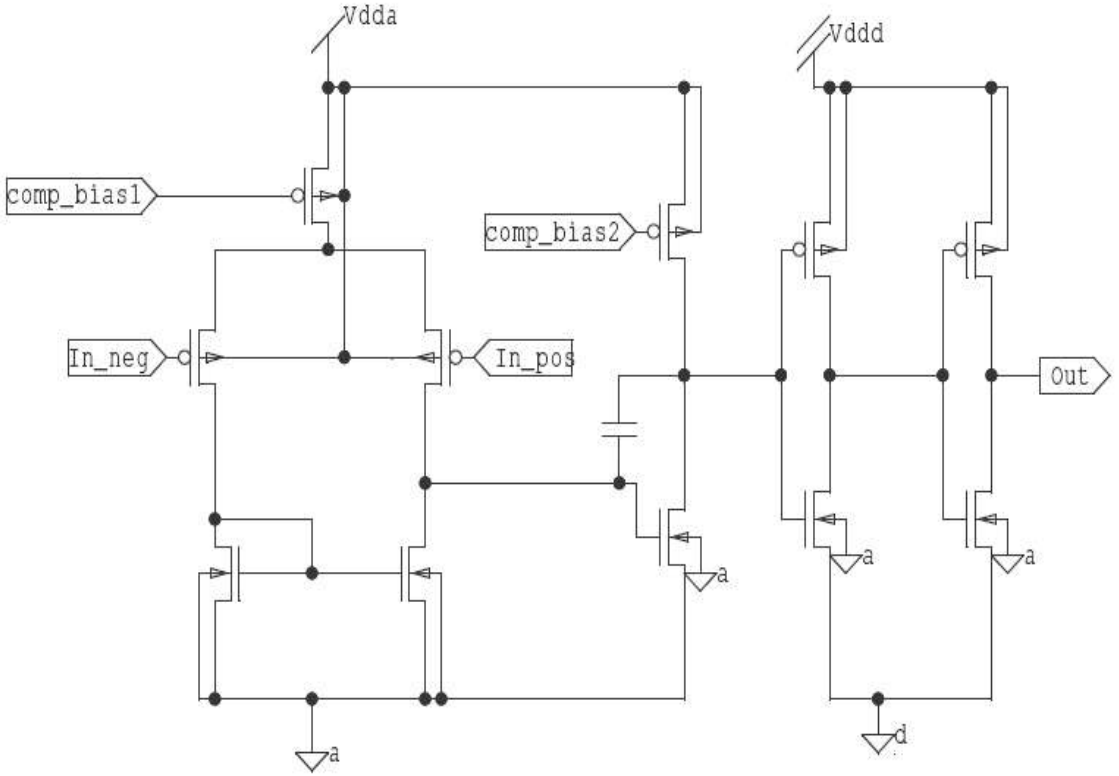
not to scale

First Prototype Measurements

- Comparator.
- Front-end amplifier.
- Counter.
- Multiple gain.
- Digitization.

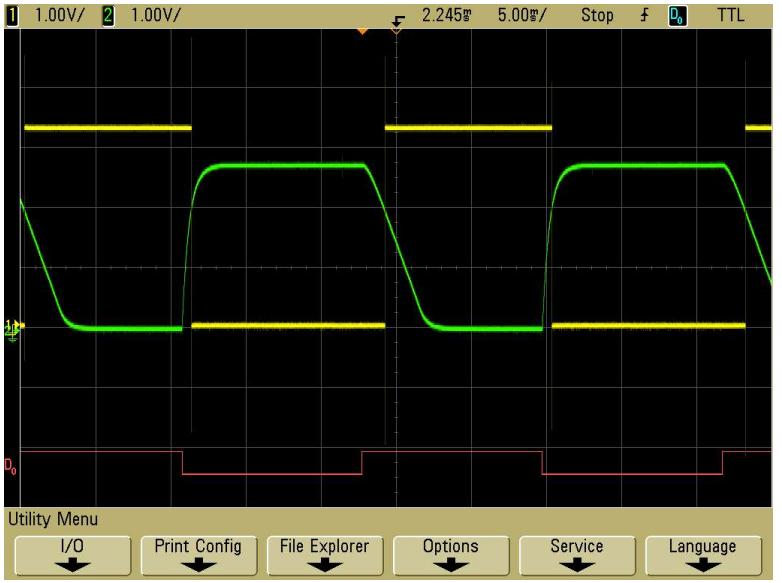


Comparator (slide 1)

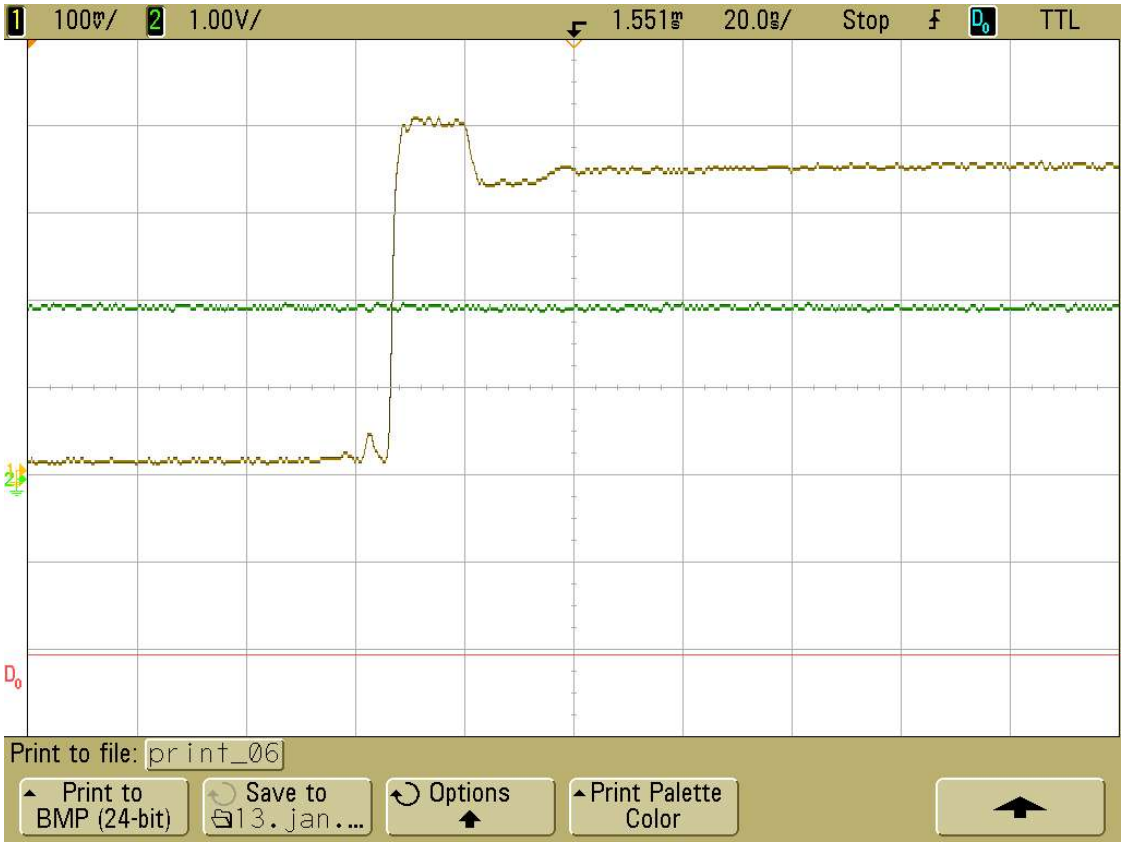


- Two important characteristics:
  - Noise.
  - Switching time proportional to voltage.

shown working with over filtered ramp signal (ramp time ~4ms here)

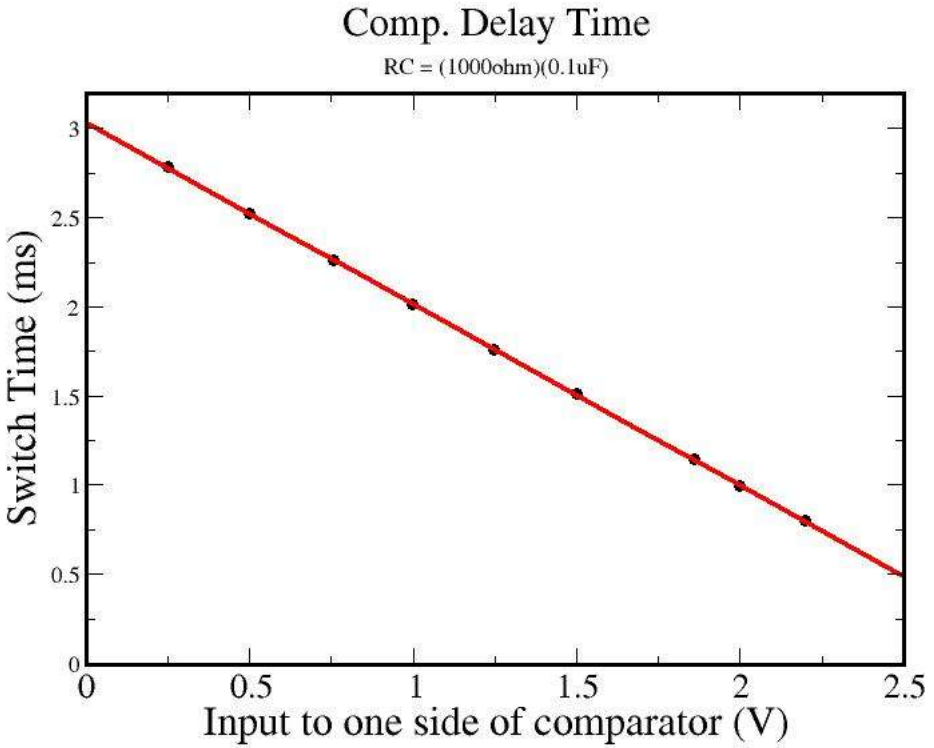


Comparator (slide 2) flipping…

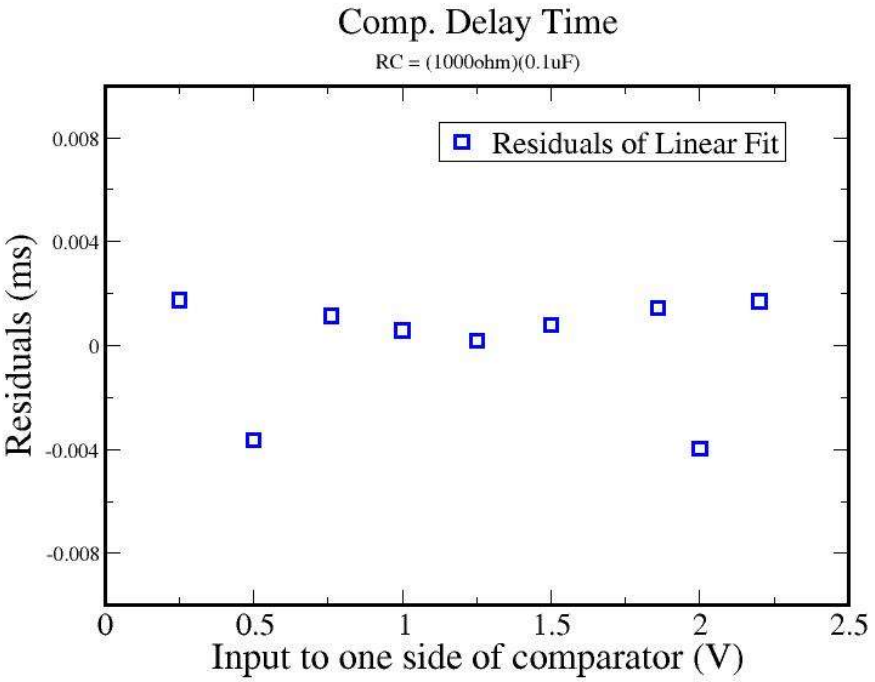


20ns scaling, sharp rise time.

Comparator (slide 3)

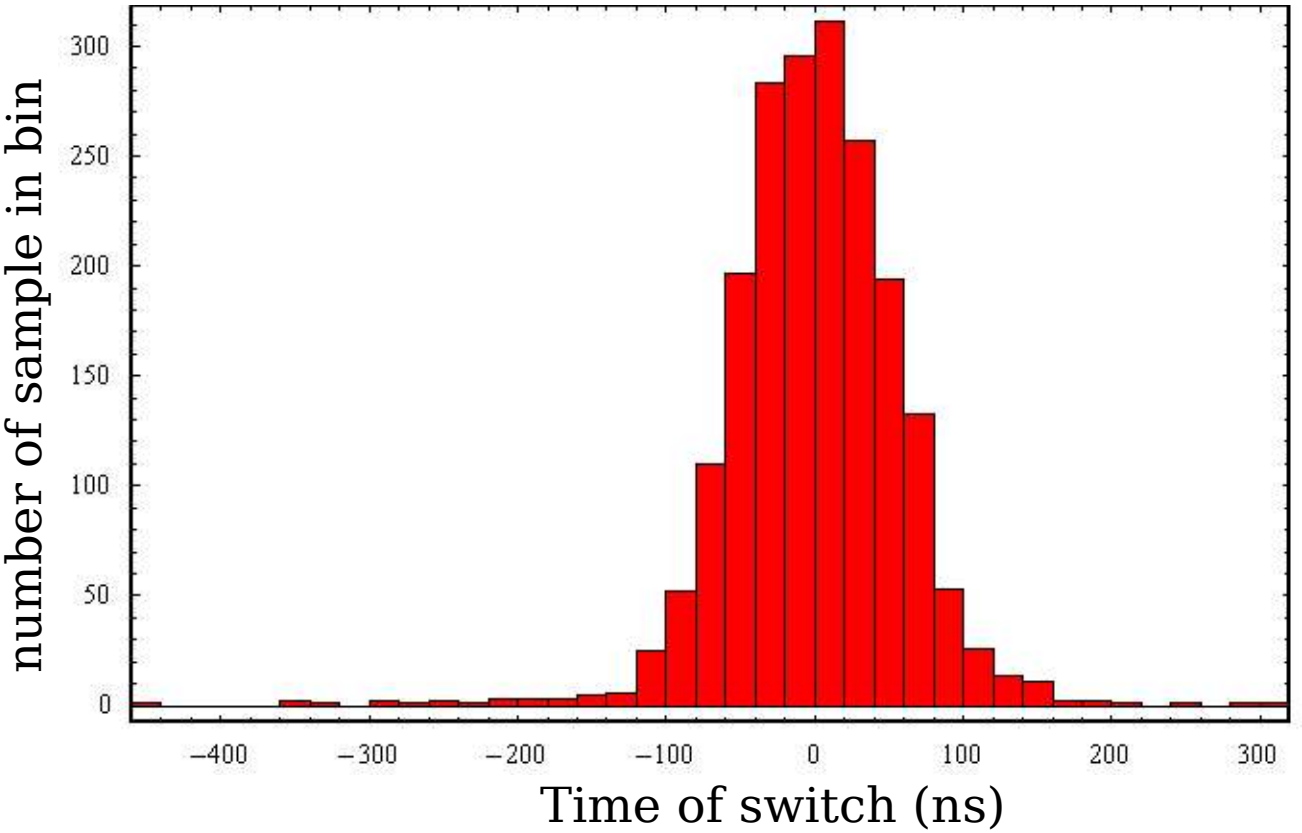


- Linearity test – time of transition vs. input voltage



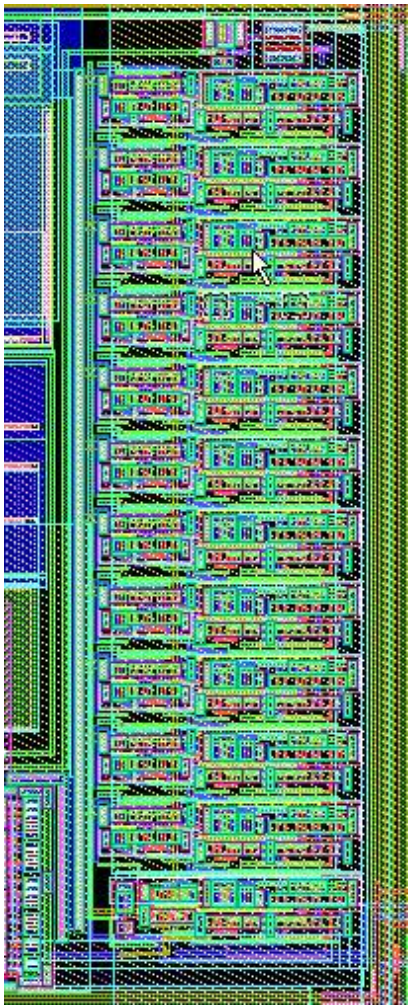
Linear to resolution of voltage source – voltage range 0.25-2.25

Comparator jitter (slide 4)



for 3 ms ramp -> σ_{time} = 57 ns or ~60 µV

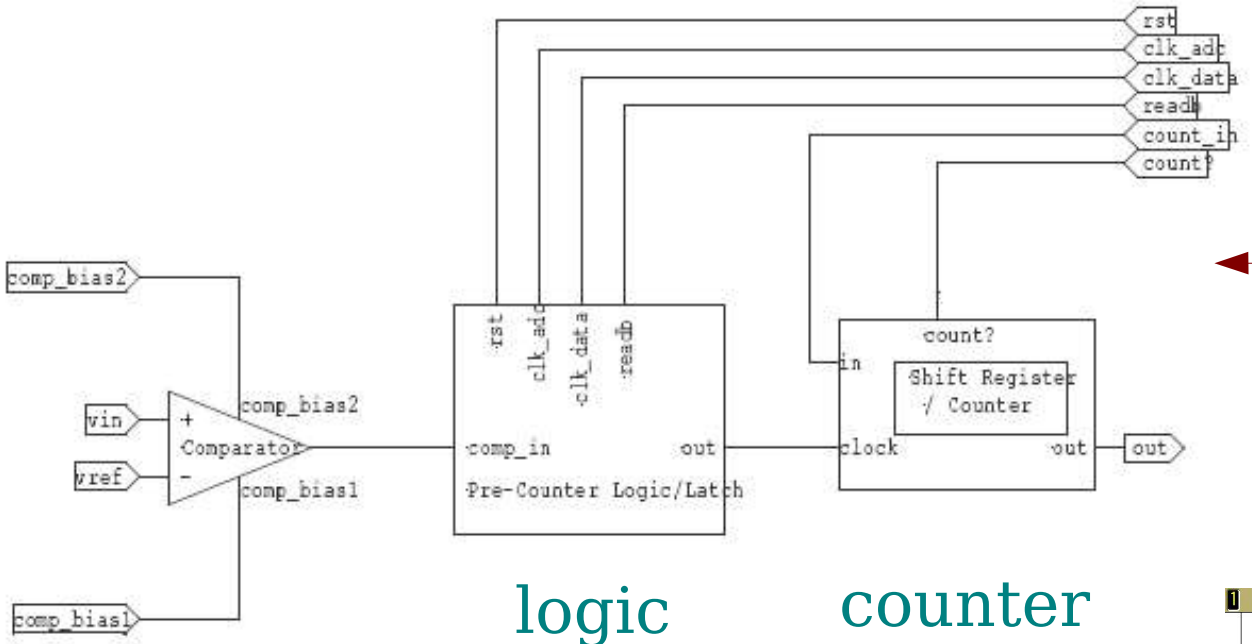
Counter



- 12-bit in-pixel.
- it counts!
- it shifts data out!
  - tested to 30 MHz (max. freq. of sig. generator)
  - Should go much faster

    (100's MHz)

Digitization test (slide 1)



← Test Circuit

comparator

logic

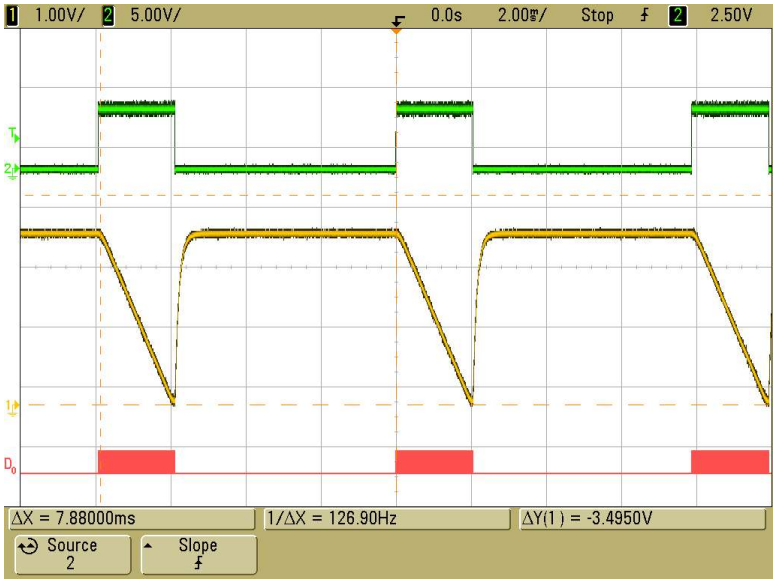
counter

waveforms
at ~125Hz,
2ms ramp →

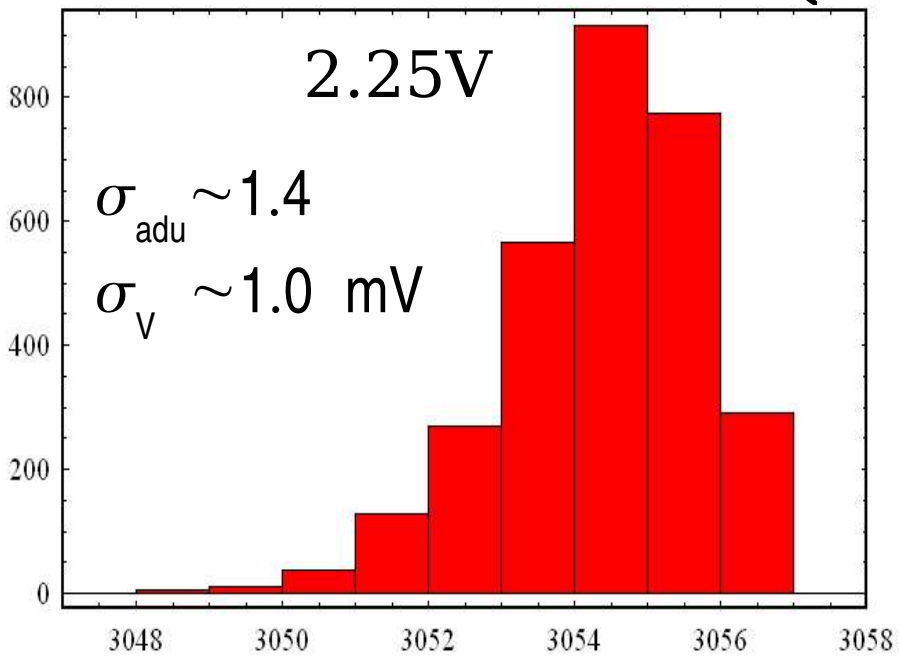
ramp ctl. →

ramp →

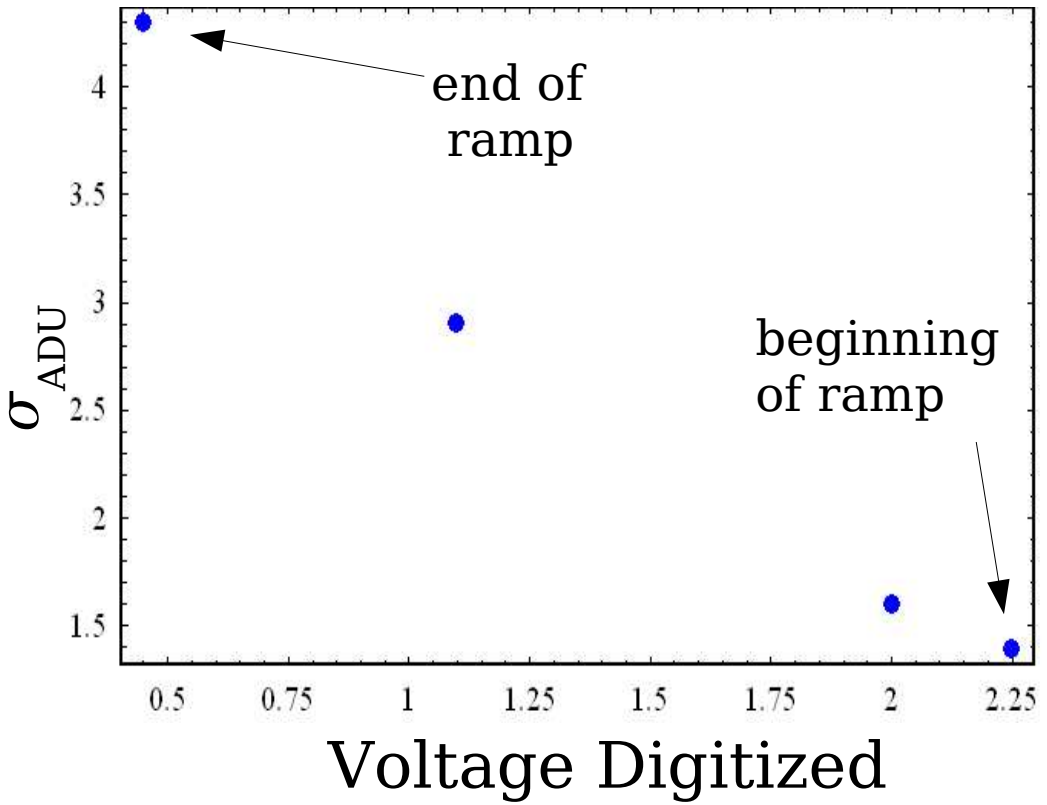
2^{12} pulses →



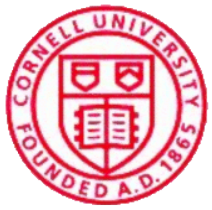
Digitization test (slide 2)



(note- 2 ms conversion ramp time)

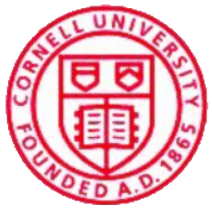


Digitization looks promising at 12-bits. More work to be done - possibly stabalizing ramp.



Next Submission (preliminary plans)

- Add enclosed layout transistors.
- Have a test structure to test correlated double sampling.
- Build larger array (e.g. 10 x 10).
- Refine pixel read out circuitry.
- Pixel addressing logic.
- Incorporate multiple gain into test pixel.



Conclusions

- A pixel architecture has been defined for in-pixel digitization.
- The first prototype has indicated that the general approach is workable.
- The scalability of the method (i.e. massively parallel conversion) must be tested.
- Tiling of the array detectors is being examined.
- Solutions for bump-bonding being pursued.

- Generally: Things are looking good. No “brick walls” yet.

Thanks

- This work has been built upon a foundation of many years of development of PAD detectors in the Gruner Group. The present PAD group includes:
  - Sol M. Gruner
  - Mark W. Tate
  - Lucas J. Koerner
  - Daniel R. Schuette
  - Alper Ercan
  - Darol Chamberlain
  - Darren Southworth
  - Thomas Caswell
  - and ... Hugh Philipp ...