X-RAY ANALOG PIXEL ARRAY DETECTOR FOR SINGLE SYNCHROTRON BUNCH TIME-RESOLVED IMAGING

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Dynamic x-ray studies may reach temporal resolutions limited by only the x-ray pulse duration if the detector is fast enough to segregate pulses. An analog integrating pixel array detector (PAD) with in-pixel storage and temporal resolution of around 100 ns, sufficient to isolate synchrotron x-ray pulses, is presented. PADs are a hybrid of a fully-depleted silicon detector for direct conversion of x-rays to charge that is electrically coupled at each pixel to a CMOS readout integrated circuit.

This thesis work first motivates PAD development by an x-ray microdiffraction study of phase transformations in self-propagating reactions at rapid heating rates when the time for nucleation is limited and concentration gradients are large. Time resolution of 55 μs and spatial resolution of 60 μm was achieved using a PAD and high flux x-ray optics. The phase progressions measured differed from similar studies at slower heating rates and provide insight into nucleation and growth in thin film samples.

Next, guidelines for a high-speed PAD at power dissipations amenable to large pixel arrays are presented. Using these guidelines, a 16×16 pixel CMOS readout was developed. The readout was hybridized to silicon detectors and combined with support electronics and flexible FPGA based control and acquisition to create an x-ray camera. The support electronics and FPGA code allowed for an exposure time down to 30 ns with 10 ns resolution, a 600 μs readout, and

buffering for 8,100 frames before a transfer to hard-disk was required. The camera was shown to resolve individual bunch trains from the Cornell University synchrotron at levels of up to 3.7×10^3 x-rays/pixel/train. Single shot intensity measurements were made with a repeatability of 0.4%-almost entirely limited by Poisson statistics. The camera remained functional after an accumulated dose of 600 kGy(Si) at the CMOS readout. Lock-in like functionality incorporated into the pixel electronics facilitated extraction of the frequency spectrum of input illumination at frequencies faster than the detector readout time. The developed camera is appropriate for experiments that explore single crystal dynamics at the Advanced Photon Source.

BIOGRAPHICAL SKETCH

Lucas Koerner was born in LaCrosse Wisconsin in 1981 and grew up in Rochester Minnesota. In 1999 he left home for Northwestern University and majored in Integrated Science Program, physics, and mathematics. He started his graduate studies in physics at Cornell University in 2003.

To my mom and dad.

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LIST OF ABBREVIATIONS

ADC	analog to digital converter
APD	avalanche photodiode
APS	Advanced Photon Source
ASIC	application specific integrated circuit
CCD	charge-coupled-device
CESR	Cornell Electron Storage Ring
CMOS	complementary metal-oxide-semiconductor
DUT	device/amplifier under test
ENC	equivalent noise charge
ERL	Energy Recovery Linac
ESRF	European Synchrotron Radiation Facility
FIFO	first-in first-out
FPGA	field-programmable gate array
FWHM	full-width at half-maximum
Gy	Gray - unit of absorbed dose
KB mirrors	Kirkpatrick-Baez mirrors
LCLS	linac coherent light source
LCLS PAD	PAD developed at Cornell for the linac coherent light source at Stanford
LYSO:Ce	cerium-doped luetetium yttrium orthosilicate
MiM	metal-insulator-metal
MMPAD	Mixed-mode PAD developed by Area Detector Systems Corporation and Cornell
MOS	metal oxide semiconductor
MOSIS	metal oxide semiconductor implementation service
NMOS	MOS transistor with n+ source and drain diffusions

PAD	pixel array detector
PCB	printed circuit board
PGA	pin grid array
PLL	phase locked loop
PMOS	MOS transistor with p+ source and drain diffusions
PSD	power spectral density
PSI	Paul Scherrer Institut
PYP	photoactive yellow protein
RF	radio frequency
RMLF	reactive multilayer foils
RMS	root mean square
RTD	resistance temperature detector
SDRAM	synchronous dynamic random access memory
SPI	serial peripheral interface bus
TOF	time-of-flight
TSMC	Taiwan Semiconductor Manufacturing Corporation
USB	universal serial bus
XFEL	x-ray free electron laser
XPCS	x-ray photon correlation spectroscopy
ZIF	zero insertion force

LIST OF SYMBOLS

CHAPTER 1

INTRODUCTION

X-ray synchrotron sources are used to probe samples at atomic length-scales. The intensity of these x-ray sources makes possible studies on *time-scales* scientifically relevant to microscopic and atomic dimensions. Yet x-ray detectors hold these studies back. This dissertation work advances time-resolved x-ray experiments through the development and utilization of high-speed detectors based on complementary metal-oxide-semiconductor (CMOS) electronics. This chapter considers exciting time-resolved science to be probed with x-rays through the discussion of example experiments. Time-resolution limits of current x-ray detector technology and ways to surpass these limits are presented. In chapter two, fast x-ray detector development is motivated by an x-ray micro-diffraction experiment that determined the phase transformation sequence of a propagating reaction front at time-scales of 55 μs. The next three chapters present a detector architecture designed to isolate individual x-ray pulses to exploit the pulsed nature of synchrotrons for time-resolution limited by the pulse-width (~100 ps) of the x-ray source. Tests confirmed the functionality of the pixel architecture. A small-area imaging camera that included high-speed low-noise and robust readout electronics was developed and tests of photon detection were obtained. The pixel included 'lock-in'-like detection which encouraged exploration of new imaging modalities. In the final chapter, further x-ray detector developments and experimental applications are considered.

1.1 X-rays and dynamics

X-ray synchrotron sources allow the visualization of structure on the atomic scale. For example, the arrangement of atoms in proteins, the orientation of crystalline grains in metals, and the presence of nanoscopic defects in otherwise perfect crystals may all be probed by x-rays. But how do materials work at atomic length scales? To determine function, the dynamics of structures must be investigated [1]. As the intensity and coherence of x-ray sources grows so too does the possibility of extracting time dependence in previously static x-ray experiments. This chapter will introduce a few x-ray experimental techniques and discuss how these techniques have incorporated dynamics. For each example the possible benefits of faster x-ray detectors that more flexibly partition time windows are discussed. Dynamic x-ray experiments completed without advanced detectors should not discourage detector development; rather, these successes prove a determination to reveal dynamics. An explosion of time-resolved studies would occur if the detector becomes a more helpful tool.

1.1.1 Example: protein crystallography

Protein crystallography uses x-rays to determine the three-dimensional arrangements of the atoms in proteins. Diffraction of x-rays of wavelength around 1 Å allows for the determination of the sample electron density to a resolution of around 1 Å (below atomic separation). To mitigate radiation damage many copies of the protein are organized into a three-dimensional periodic lattice, or crystal, with dimensions typically on the order of a hundred microns. A fraction of the x-rays incident upon the sample elastically scatter and interfere constructively to form Bragg spots that measure the Fourier transform of the electron

density of the sample. Complex computer programs are used to develop a map of the protein structure from the measured diffraction. Proteins often remain active when packed into a crystal since most of the molecule is surrounded by solvent while only a few residues contribute to packing forces [2].

The energy landscape of protein molecules are complex and motions occur over many orders of magnitude in time. Bourgeois *et al.* used Laue protein crystallography to study the structural dynamics of myoglobin after photodissociation (via a laser pump pulse) of carbon monoxide from the heme iron and found the relaxation process to follow time-scales from picoseconds to milliseconds [2]. Motions local to the heme were found to occur promptly after photolysis (< 3 ns), other, more global, motions propagated from the active site in 300 ns, and final relaxation required 3 ms. Similarly, the motions associated with the photocycle of photoactive yellow protein (PYP) have been studied from 10 ns to 100 ms [3]. These time scales are accessible by the detectors that will be described in this dissertation.

For these experiments, the time coordinate was set by the delay between a laser pulse that initiates the dynamics and a single x-ray pulse probe to measure the dynamics. This stroboscopic technique is commonly referred to as "pump-probe". To extract a single pulse from the synchrotron (required to achieve time-resolution without a fast x-ray detector) the experimenters in [2] used three x-ray shutters. The multiple shutter system included an ultrafast chopper wheel that rotated at a frequency of 445 Hz. Furthermore, the European Synchrotron Radiation Facility (ESRF) was required to run in a dedicated single-bunch mode that produced x-ray pulses every 2.99 μs with a width of 62 ps [4].

A detector sufficiently fast to electronically shutter all but a single pulse from the synchrotron would simplify and increase the flexibility of the experiments

described above. The detector described in this dissertation was designed to shutter signal electronically and to record multiple images with in-pixel storage before detector readout.

Laser-pump x-ray-probe experiments have accomplished nanosecond and faster time resolution for studies of photo-active proteins [5]. Yet, such success should not limit the imagination. Detector development will be required to study other trigger mechanisms. Evolution of intermediate complexes in an enzyme catalyzed reaction and protein responses to pressure jumps or applied voltage [6] could all be studied dynamically. If these examples are not reversible or do not trigger cleanly, their study may only be feasible with a flexible, fast detector able to acquire multiple temporal windows in succession.

1.1.2 Example: x-ray photon correlation spectroscopy

X-ray photon correlation spectroscopy (XPCS) probes a sample with a coherent x-ray beam to produce a speckled diffraction pattern. The time fluctuations of the speckles correspond to the characteristic fluctuation times of the scattering elements of the sample. Studies of equilibrium fluctuations at atomic length scales, for example the diffusion of atoms in a solid, require a coherent probe such as that used by XPCS [7]. At the ESRF an XPCS experiment has studied the dependance of diffusion of atoms in an $Cu_{90}Au_{10}$ solid solution upon the local neighborhood. This study was the first to reach atomic length-scales (4.5 Å) using XPCS and found correlation times from a few hundred to 5,000 s. This experiment utilized a large-area directly illuminated CCD detector [8]. Other experiments have reached correlation times of $< 1\,\mu$s at a length-scale of $110\,\mu$m using a single channel avalanche photodiode [9].

Length-scale and accessible correlation time are inversely related in an XPCS

experiment. This is explained by consideration of the coherent scattering volumes as spheres of homogenous electron density. The Guinier expression for diffraction by a sphere gives the scattering amplitude to be proportional to $1/q^3$, where q is the momentum transfer [10]. At a spatial resolution of d ($d = 2\pi/q$) the scattered intensity is thus proportional to d^6 [11]. The large intensity fall-off versus spatial resolution explains why accessible correlation times are inversely related to length-scale.

Future x-ray sources are anticipated to produce a dramatic increase in coherent flux from what is available at synchrotron based x-ray sources. Specifically, a two to three orders of magnitude increase in coherent flux is anticipated at the proposed Energy Recovery Linac (ERL) at Cornell over the Advanced Photon Source (APS) [12]. For XPCS experiments, increased coherent flux subsequently reduces the accessible correlation times by the square of the increase in coherent flux [12]. These gains could allow the study of glasses and colloidal suspensions [12]. However, the realization of this vast improvement in XPCS will require sufficiently fast detectors. The signal-to-noise advantage gained in XPCS through the use of two-dimensional area detectors, as opposed to point detectors, is well established [13]. However, for standard area detectors, the minimum correlation time accessible in XPCS is limited by the time required to read-out a frame. Yet this does not have to be the case if the detector pixel is designed to partition time windows flexibly. The temporal flexibility of the detector described in this thesis was shown to allow access of correlation times far shorter than the frame readout-time.

1.1.3 Example: crystalline dynamics

DeCamp and coauthors summarized synchrotron studies of dynamics, at nanosecond or faster time scales, in crystalline materials [14]. Solid crystalline materials studied at the nanosecond to picosecond regime with x-rays have revealed, for example, the time dependence of the shift from elastic to plastic deformation [15], the acoustic dispersion relation within strained single crystals [14], and the propagation of ferroelectric polarization domain walls [16]. Consider the shift from elastic to plastic deformation. Non-reversible plastic flow requires the creation and motion of dislocations; perfect crystals with fewer defects and slower defect velocities should require a longer time for the transition from elastic to plastic flow. Loveridge-Smith *et al.* showed this by laser-induced shock of perfect crystals of silicon and copper [15]. A streak camera was used to track the temporal changes of the lattice spacing through the Bragg scattering angle. The copper dislocation velocity was known to be 6-7 orders of magnitude faster than that of silicon. The disparity of dislocation velocities was shown as copper flow became plastic on subnanosecond time-scales while the response of the silicon crystal remained elastic at all time-scales measured. In this experiment the streak camera allowed access to subnanosecond temporal resolutions but was limited in terms of temporal dynamic range. The detectors described in this dissertation, while not as fast as streak cameras, could expand the dynamic range of the time-scales accessible to reach the millisecond or microsecond regime necessary to study the silicon elastic to plastic transition.

The propagation of ferroelectric domain walls provide an opportunity to study phase transformations in the solid state [17]. Ferroelectric materials have emerged as a candidate for low power, fast switching random access memories. An applied external field initiates a switch of the polarization direction,

domains of which nucleate and grow. Grigoriev *et al.* synchronized the application of an external field to synchrotron x-ray pulses to study the propagation of polarization domains in a $Pb(Zr_{0.45}Ti_{0.55})O_3$ (PZT) ferroelectric capacitor [16]. Polarization switching caused expansion or contraction of the atomic spacings (piezoelectric effect) which was detected by a change in scattering angle of the Bragg diffraction. The experiment tracked the domain wall motion over a distance of 14 μm and times up to 350 ns to deduce a domain wall velocity of 40 m/s, much below the elastic limit but in agreement with simulations [16]. These experiments utilized a single-point avalanche photodiode (APD). The APD was sufficiently fast to resolve single bunches from the synchrotron but, since the APD is a single pixel detector, multiple acquisitions were required with the detector positioned to detect different scattering angles. If the Bragg condition is satisfied throughout the transitions (sufficient incident x-ray beam divergence and a small change in the scattering angle), a fast area detector could remove the need for translations and allow capture of the data in one-shot. Further, an area detector could record multiple Bragg reflections simultaneously [18].

Similar dynamics occur in polycrystalline materials. These materials, which include most metals, consist of multiple crystallites with arbitrary orientations. As will be seen in chapter 2, experiments that study dynamics of polycrystalline materials benefit from an area detector to detect the diffraction from crystallites of unknown orientation.

1.1.4 Example: direct imaging

Direct x-ray imaging allows for interrogation of samples that are optically dense due to excess scatter or absorption in the visible regime. A specific important

question to be studied by direct x-ray imaging is the dynamics of complex fluid flow. High-speed fluid jet breakup is still not fully understood.

Direct imaging passes an x-ray beam through the sample while an in-line detector records the transmitted beam. The detector to sample distance determines the dominant contrast mechanism. At short distances sample absorption dominates. With sufficient x-ray beam spatial coherence and detector to sample distance the gradient of the phase shift induced by the sample provides additional contrast. Contrast from phase shifts, referred to as differential phase contrast imaging, often exceeds that from absorption. The phase-shift term of the complex index of refraction of materials at x-ray energies may exceed the absorption term by a factor of 1000 [19]. Further, differential phase contrast imaging preferentially extracts edges due to the dependance on the phase-shift gradient.

A pixel array detector (PAD) from the Cornell group has been used to image the mass distribution of diesel sprays and gasoline sprays with x-rays at microsecond temporal resolution and 150 μm spatial resolution [20, 21, 22]. Further work used the experimental data of gasoline fuel sprays to confirm numerical simulations of the fluid breakup [23]. These experiments studied highly reproducible sprays; final results were an average of many repetitions of the spray.

Experiments at the APS have imaged non-repetitive turbulent flows [24]. This work used a detector system with a field of view of 1.36×1.71 mm^2 that consisted of a fast cerium-doped luetetium yttrium orthosilicate (LYSO:Ce) scintillator crystal the image from which was redirected by a 45° mirror and magnified by ×5 with a microscope objective onto a fast camera. A high-speed shutter, a special synchrotron operating mode, 'hybrid-singlet,' and a 1 μs minimum camera exposure time allowed for a snapshot of the fluid flow that was not blurred

by the flow velocity of 60 m/s. The velocity of the flow was extracted by acquisition of a double-exposure (the detector was exposed to two x-ray pulses separated by 3.62 μs) and calculation of the autocorrelation of the resultant image. The LYSO:Ce scintillator decay-time was sufficiently rapid (40 ns 1/e [1]) to not hinder time resolution. The imaging system had a spatial resolution with a ~2 μm full-width at half-maximum which allowed extraction of fine spatial features within a small-viewing area close to the spray injector. The system efficiency was estimated to be only a few percent [25]; PAD detectors efficiencies at the 13.3 keV x-ray energy used exceed 80%. Efficiency would be an important consideration if the system to study is radiation sensitive. More significant to detector considerations, the flows studied were not reproducible. Flow evolution would be revealed most completely by a detector with in-pixel storage that allows the capture of multiple sequential snapshots with sub-microsecond spacing. A direct imaging experiment appropriate for a PAD would: require high-efficiency, image non-repetitive objects, require a larger field of view than used in the turbulence experiment described above, and contain spatial features no smaller than the pixel size of the PAD.

1.1.5 Summary of experimental examples

Knowledge of dynamics at the nanoscale elucidates function. Successful studies of dynamics with x-rays have been performed, for example, in the areas of protein crystallography, x-ray photon correlation spectroscopy, crystalline materials, and direct x-ray imaging of complex fluid flow. Instrumentation has generally limited these studies to reversible dynamics initiated by laser pulses. With time-resolution accessed via electronic control of a fast area detector studies of

[1] www.omegapiezo.com

non-reversible dynamics initiated by a much more diverse array of triggers are possible.

1.2 X-ray sources

X-ray synchrotron sources produce x-rays when electrons or positrons are accelerated by magnetic insertion devices. Tight bunches of the charged particles are maintained by radio frequency (RF) fields while the particles circle the synchrotron ring. The temporal spacing between bunches, t_{bunch}, is set by the configuration of the RF fields and the population of charged particles into the RF fields. The temporal width of x-ray pulses, w_{bunch}, is limited by the longitudinal length of the particle bunch. A cartoon of a synchrotron ring with traveling electron bunches is shown in Figure 1.1. The timing parameters at common synchrotron facilities are compiled in Table 1.1. From this table certain bunch timings are extracted to motivate the work in this dissertation. Of course, the requirements vary dramatically depending upon the synchrotron considered. In particular, this work has focused upon the bunch-to-bunch spacing during standard operation at the APS ($t_{bunch} = 153\,\text{ns}$), two-bunch mode at the Advanced Light Source ($t_{bunch} = 328\,\text{ns}$), and 16-bunch mode at the European Synchrotron Radiation Facility ($t_{bunch} = 176\,\text{ns}$).

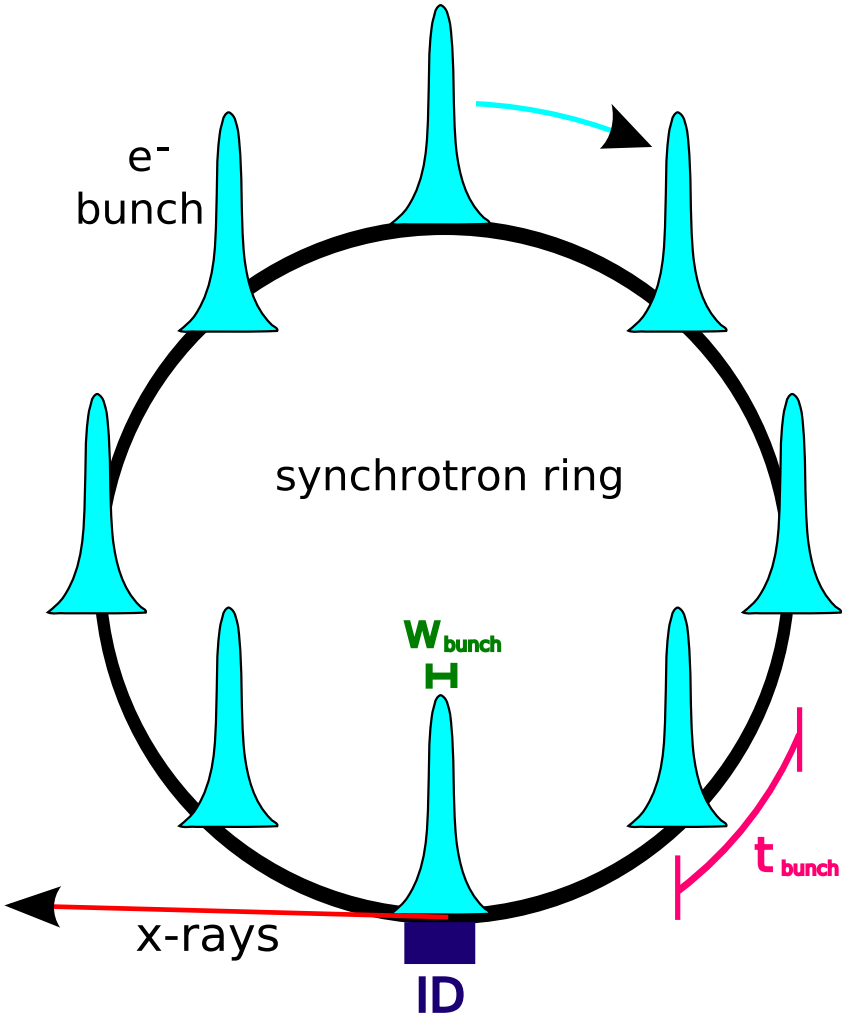


Figure 1.1: A cartoon of a synchrotron ring with eight electron bunches (shown in teal) orbiting the ring. The critical timing parameters, w_{bunch} and t_{bunch} are labeled. A magnetic insertion device (ID) is drawn in blue. The cartoon is not to scale; synchrotron rings are around 1 km in circumference. Temporal quantities are represented as spatial dimensions; the charged particles in a synchrotron move at highly relativistic speeds such that distances are related to time by the speed of light.

Table 1.1: Timing parameters of fill patterns at common synchrotron x-ray sources and the under-construction European XFEL. Common non-standard operating modes used for timing experiments are listed when applicable. APS - Advanced Photon Source, Argonne, IL, USA. ALS - Advanced Light Source, Berkeley, CA, USA (1 - multibunch mode; 2 - two-bunch mode). CHESS - Cornell High Energy Synchrotron Source, Ithaca, NY, USA. ESRF - European Synchrotron Radiation Facility, Grenoble, France (1 - standard operation; 2 - 16-bunch mode). EXFEL - European XFEL at DESY, Hamburg, Germany. NSLS - National Synchrotron Light Source, Upton, NY, USA (1 - standard operation; 2 - five bunch mode; 3 - single bunch mode). SLS - Swiss Light Source, PSI, Switzerland. SPring8 - Super Photon Ring, Hyōgo Prefecture, Japan (1 - 'A-mode': 203 bunches; 2 - 'C-mode': 11 bunch train $\times$ 29; 3 - 'D-mode': 1/14-filling + 12 bunches). At CHESS the synchrotron ring is populated with nine trains of five bunches. Closely spaced bunches, separated by 14 ns, compose the trains. For each individual bunch the longitudinal length is w_{bunch} = 65 ps (σ). C-mode at Spring-8 is filled with 29 trains of 11 bunches. The bunches within each train are separated by 1.966 ns. For CHESS and Spring-8 'C-mode' the bunch spacing reported in the table is that of the trains.

Source	Bunch Spacing	Bunch Width
	t_{bunch}	w_{bunch}
ALS (1)	2 ns	65 ps
ALS (2)	328 ns	65 ps
APS [26]	153 ns	20 ps
CHESS	280 ns	5 bunch train
ESRF (1)	2.82 ns	20 ps (RMS)
ESRF (2)	176 ns	48 ps (RMS)
EXFEL [27]	200 ns	100 fs
NSLS (1)	18.9 ns	290 ps (2σ)
NSLS (2)	94.5 ns	290 ps (2σ)
NSLS (3)	567.2 ns	290 ps (2σ)
SLS	1.88 ns	N/A
SPring-8 (1)	23.6 ns	70 ps (FWHM)
SPring-8 (2)	145.5 ns	11 bunch train
SPring-8 (3)	342.1 ns	70 ps (FWHM)

Setups at the APS have yielded 3×10^{15} photons/s with a 2% bandpass or 2×10^{13} photons/s with a 1.4 eV bandpass. These numbers resulted in 4.6×10^{8} photons/pulse and 3.1×10^{6} photons/pulse for high and low-bandpass config-

urations, respectively. The fraction of photons incident on the sample that proceed to the detector depends on a vast array of experimental parameters. Yet, it is clear that for in-line imaging ($\sim$50% to detector) and single crystal diffraction ($\sim$1% or more to detector) 10^4 to 10^6 photons to the detector in a single pulse is possible.

Some time-resolved x-rays studies, including the shock driven elastic-to-plastic transitions discussed above, have utilized tabletop x-ray sources. A common approach to create a tabletop source has used a pulsed terawatt laser to produce a plasma in a metal that subsequently ejected x-rays. The pulse-width of these sources can be sub-picosecond but the collimation and spectral purity is limited when compared to synchrotron sources. The possible x-ray energies are confined to the line emission of metals, such as tantalum, titanium, tungsten, copper, iron, and molybdenum [28]. Since the repetition rate of the pulses is limited to around 10-1000 Hz, and is more configurable than the synchrotron, less speed is demanded from the detector system.

1.3 X-ray detectors and the basics

In this section x-ray area (a two-dimensional grid of pixels) detectors currently in use at synchrotron x-ray sources are discussed. The section begins with an introduction to charge-coupled-device (CCD) detectors made x-ray sensitive by incorporation of a phosphor that stops x-rays and produces optical photons in front of the CCD. These devices are the predominant detector technology in use today at synchrotrons. This example is used to motivate work on technologies with fewer inherent limitations. The time-resolution of each architecture is an aspect of focus.

1.3.1 Phosphor coupled charge-coupled-devices

Area x-ray detector technology made a giant leap in the early 1990's with the development of charge-coupled-device (CCD) detectors that reached signal-to-noise ratios near one for x-ray detection without image intensification [29]. CCDs measure the position and quantity of charge deposition from an image in an array of pixels by sequential transfer of charge packets to an amplifier at the edge of the array. The most common application of CCDs to x-ray imaging has used a detector system that consists of a phosphor to stop x-rays and convert the energy to visible light, a demagnifying optical element of either a lens or fiber-optic taper, and a CCD that detects the visible light.

The detection process begins with x-ray conversion in a phosphor with the energy carried converted to optical photons. A typical phosphor, Gd_2O_2S:Tb, has an energy efficiency around 15% and emits in the green [30]. The detector area required for x-ray diffraction experiments generally exceeds the size of commercially available CCD chips. Thus, the light output from the phosphor is demagnified before reaching the CCD using lenses or tapered fiber optic bundles. Fiber-optic tapers are preferred as their efficiency approaches limits set by the brightness theorem (product of size and divergence remains fixed). The optical light is detected by the CCD; each optical photon that converts in the silicon of a CCD produces a single electron-hole pair. At the end of the exposure the photo-charge is transferred in a serial fashion to output amplifier(s) and digitized.

Efficient phosphors may direct 10% of the x-ray energy toward the CCD chip–given this assumption a 10 keV x-ray produces an average of 430 green photons collected by the fiber-optic taper. With a 3.3:1 demagnification ratio fiber-optic efficiency has been reported to be 13% [30] so that 56 photons are

incident upon the CCD. Standard CCD detection efficiencies are 30% [30] such that, in this model, a 10 keV x-ray produces an average of 17 e^-. The noise associated with readout of a CCD pixel is around 10 e^- at 50 kHz pixel-rate [31] so that the detector chain reaches a signal-noise ratio of approximately one. The above processes are average outputs; the fluctuation in electrons per x-ray may be around 40% of the average value [31].

The serial nature of CCD readout generally holds full-chip readout times to seconds. Frame transfer CCDs use half of the pixels for image acquisition while the other half are used for data storage. By a quick shift of an acquired image into a data store area another acquisition may begin rapidly. A frame transfer of 1.6 ms is reported in [32] but readout requires 1.9 s and limits the minimum exposure time. Phosphor after-glow also limits time resolution. For most phosphors emission decay switches from exponential to algebraic fall-off tens of milliseconds after excitation. After-glow can prevent the detection of low-level signals in a rapidly changing image and cause a slow buildup of background [30].

Area CCD x-ray detectors coupled to phosphor screens have successfully developed the field of protein x-ray crystallography; yet, the adaptation of components envisioned for optical systems to the x-ray regime seems to have hit a limit of further development. Certainly, time-resolution is severely constrained with phosphor-coupled CCDs.

1.3.2 Detection in semiconductors

Further discussion of x-ray detector technology requires an overview of photon conversion in semiconductors. This discussion is general to semiconductors but specific quantities will be drawn from silicon. Other semiconductor materials have desirable properties for x-ray detection but the quality of and industrial

experience with silicon makes its use significantly more practical. An excellent review of compound semiconductor radiation detectors is given in [33].

Electron-hole pairs are created in a semiconductor when a photon converts. Conversion is a statistical process that depends on the electron density and thickness of the material and the photon energy. A mean quantity of charge, N_{eh}, is created. The value is given as, $N_{eh} = E_{ph}/E_{pair}$, where E_{ph} is the photon energy and E_{pair} is the electron-hole pair creation energy of the material [30]. E_{pair} is 3.65 eV for silicon at energies above 1.5 keV [34][2]. Inherent energy resolution of the conversion process is set by statistical fluctuations of the number of electron-hole pairs produced. The fluctuations are due to the division of the photon energy between production of mobile carries and excitation of the crystal lattice. Since the energy for lattice excitation is less than the energy for electron-hole pair creation the statistics of carrier generation are better than anticipated from Poisson statistics by a value referred to as the Fano factor [34]. For silicon the measured Fano factor is, $F = 0.1$, such that the standard-deviation of charge created is given as $\sqrt{FE_{ph}/E_{pair}}$. The energy resolution is then given as $E_{pair}\sqrt{FE_{ph}/E_{pair}}$ [34]. The root-mean-square (RMS) fluctuations of the charge produced in silicon by a 10 keV x-ray are 0.60% of the mean; far superior than the fluctuations of optical photons described earlier for indirect x-ray imaging configurations.

Time resolution inherent to semiconductor detectors is determined by collection of charge carriers. Rapid collection requires that the conversion volume of the semiconductor be fully depleted, such that an electric field is present throughout, to drift the created charge to measurement electrodes. The probability of stopping an x-ray, or detector efficiency (QE), increases with thickness,

[2]Photon energy needs only to exceed the semiconductor band-gap for creation of a single electron-hole pair (1.12 eV for silicon), hence the one electron per visible photon cited in the earlier discussion.

d, as $QE = 1 - e^{-d/L_{1/e}}$ where $L_{1/e}$ is the attenuation length of the material the x-ray energy in consideration. The time for collection also increases with detector thickness. Hence, efficiency is exchanged for time-resolution and vice versa.

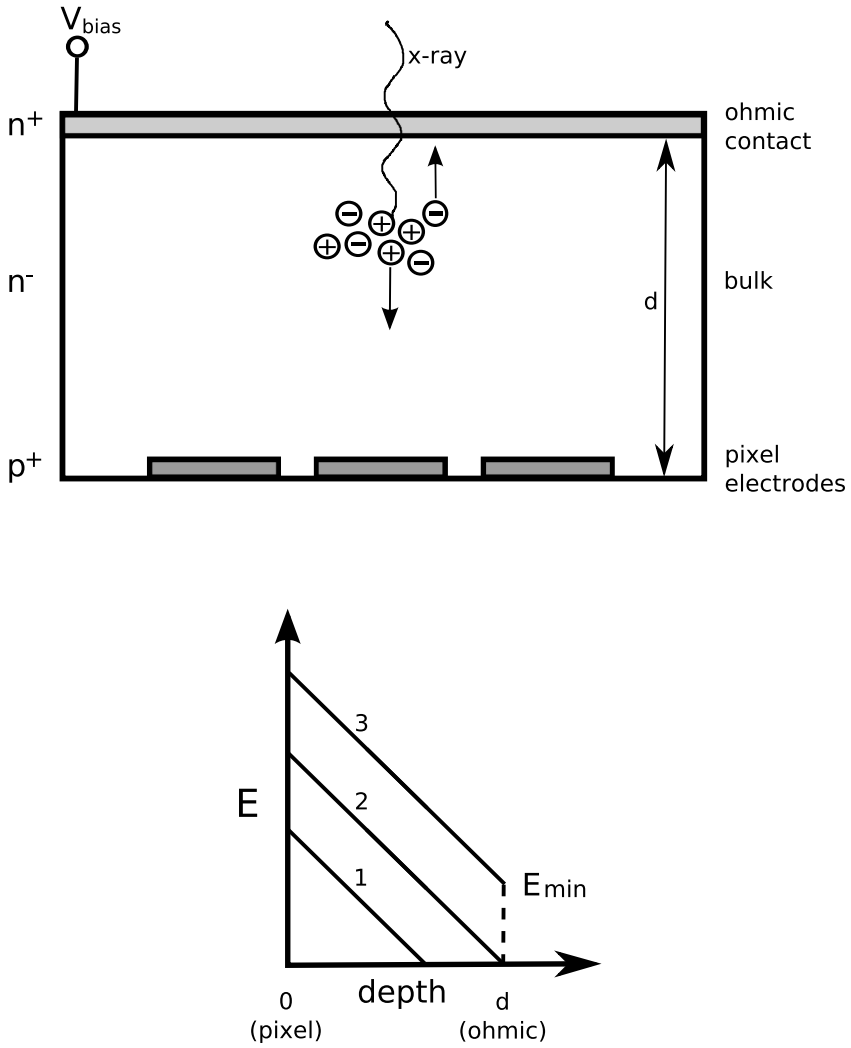


Figure 1.2: On top a schematic of a pixelated semiconductor detector layer. X-rays that convert in the bulk create electron-hole pairs. An applied potential, V_{bias}, creates a field that drifts electrons to the n^+ ohmic contact and holes to the p^+ pixel electrodes. Bottom, a plot of the electric field versus depth within the detector bulk. Applied V_{bias} increases from field profile 1 to 3. Profile 1 shows a detector that is not fully depleted as a zero-field region exists. Profile 2 is for a detector with an applied voltage just sufficient to fully-deplete the bulk. Profile 3 represents an over-depleted detector. Adapted from [34].

Next, with reference to Figure 1.2, simple approximations are used to estimate the time-resolution inherent to charge collection. At a voltage, V_{dep}, specified by the thickness and resistivity of the semiconductor the detector is depleted of mobile charge and has an electric field throughout the entire thickness. With an applied voltage, V_{bias}, past that required for depletion, the minimum field found at the backside ohmic contact is given as $E_{min} = V_{ob}/d$, where $V_{ob} = V_{bias} - V_{dep}$. The electric field grows linearly with distance from the ohmic contact until the maximum field is reached at the pixel electrode. If the field is assumed constant at its minimum value, E_{min}, a bound of the maximum collection time is calculated as $t_c = d^2/(\mu V_{ob})$, where μ is the carrier mobility and d is the thickness of the detector[3]. At fields greater than 10^5 V/cm carrier velocity saturates at around 10^7 cm/s (100 μm/ns) and electrons acquire enough energy to eject other electrons during lattice collisions[4] [34]. For an overbias of 200 V a maximum bound on the hole collection time, t_c, from a 500 μm thick detector is 28 ns (carrier velocity of $2{\times}10^6$ cm/s). The minimum collection time, constrained by the saturated velocity, is 7 ns. These estimations suggest that charge collection in a silicon detector sufficiently thick for efficient x-ray stopping does not prevent temporal resolution at synchrotron single bunch separation. Figure 1.3 presents stopping efficiency and hole-collection times versus thickness for a silicon detector. This figure uses more complete calculations of collection times that consider the detector built-in voltage and the change of the electric field throughout the detector thickness.

[3] Precisely, collection time is the time between photon conversion and the conclusion of signal current at the pixel electrode. Due to induced charge, signal current is present at the pixel electrode as soon as charge moves in the semiconductor and continues for the duration of the charge collection time (Ramo's theorem) [35]. For this discussion the worst case scenario of conversion in the bulk at a position furthest from the pixel electrodes has been assumed.

[4] In this work the high-field carrier avalanching regime is avoided.

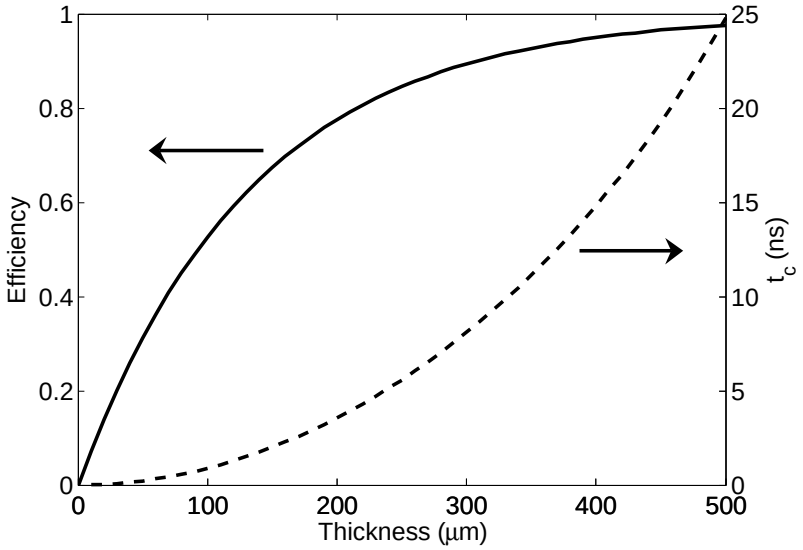


Figure 1.3: Hole collection time, t_c, (dashed) and efficiency for detection of 10 keV x-rays (solid) versus silicon detector thickness. Assumed is an n-type silicon 7.5 kΩ·cm detector with an applied voltage of 250 V.

Spatial resolution of semiconductor photon detection is primarily limited by the diffusion of charge in the direction orthogonal to drift. The diffusion constant is given by the Einstein relation as $D = (kT/e)\mu$, with k the Boltzmann constant, T temperature, e electron charge and μ the carrier mobility [36]. The diffusion length, $\sqrt{2Dt_c}$, for a collection time of 25 ns is 7.9 μm at room temperature. Fiber-optic coupled CCDs have worse response to a point illumination source. The spread of a point source was measured to have a full-width at half-maximum (FWHM) of 80 μm and to have long range tails (non-gaussian decay) that resulted in a full width at 1/1000 maximum of 450 μm [37].

Direct detection in semiconductors has been shown to be efficient, sufficiently fast for single-bunch temporal resolution, to have a spatial resolution better than 10 μm, and to have an excellent inherent signal-to-noise ratio. Next, beginning with directly illuminated CCDs, we present common detectors based

on direct x-ray conversion in semiconductors. Discussion of CMOS readout chips hybridized to semiconductor detectors, a configuration referred to as a pixel array detector (PAD), follows. The basic pixel architectures used for CMOS readout chips of PADs is compared. Finally, streak cameras and avalanche photodiodes, two unique x-ray detectors designed primarily for fast response, are presented and the advantages and disadvantages with respect to a fast PAD are considered.

1.3.3 Direct illumination CCDs

Direct x-ray conversion in a CCD yields an excellent signal-to-noise ratio since the number of electrons produced exceeds CCD read-noise by factors in the hundreds. Since the CCD surface oxide is sensitive to radiation damage and absorption of photons by the clock distribution lines reduces efficiency, direct x-ray illumination of CCDs is often from the backside. For efficiency at x-ray energies above a few keV a thick substrate is necessary. The substrate must be fully-depleted for sufficient spatial resolution, which requires that the CCD is manufactured on high resistivity silicon. Fully-depleted thick CCDs (300 μm or thicker) have been built for infrared astronomical work and have migrated to the synchrotron community [38, 39]. Reverse-illuminated CCDs with less stopping power are available from Princeton Instruments (Trenton, NJ) with $QE = 20\%$ at 8 keV, a 15 electron RMS readout noise, and a frame readout time of 1 second for a 1340×1300 array of 20 μm^2 pixels[5]. These devices are the instrument of choice for low-noise large-area imaging especially with soft x-rays [40]. A custom fully-depleted 600 μm thick CCD with a companion high-speed digitizing integrated circuit has been designed capable of 200 frames per second

[5]PI-MTE: 1300B

readout [39]. Significant increases in CCD readout speed should not be anticipated. Clock-rates are limited by the time required for sufficient charge transfer efficiency, RC constants of clock lines, and constraints on power dissipated for clock line switching [41]. Direct detection in silicon allows for excellent noise and spatial resolution, but the serial nature of CCD readout severely limits time-resolution for a 2D area detector.

CCD detectors optimized for optical detection have been designed with in-situ image storage for capture rates of up to one-million frames-per-second with a record length of 103 frames [42]. A slanted array of CCD register elements acted as in-situ memory for each pixel to rapidly store images. The first implementation was illuminated from the front-side and had a limited fill-factor of 13% due to the area consumed by the memory elements [42]. Later developments modified the approach for backside illumination with an electric potential configuration to maximize fill-factor [43]. Future modifications are predicted to yield frame rates upwards of 10-20 million frames-per-second. Photons not absorbed in the 30 μm thick substrate may convert in the pixel memory areas and corrupt stored data [43]. Memory corruption with x-rays plus the limited charge handling capacity of 10,000 electrons per pixel makes application of this high-speed architecture to x-rays technologically challenging.

1.3.4 Pixel array detectors

Pixel array detectors consist of a high-resistivity semiconductor detector layer electrically coupled at each pixel via bump-bonds to a readout application specific integrated circuit (ASIC) [44]. The readout ASIC is fabricated through the same commercial CMOS processes that have been used for the production of computer processors, and as such, economies of scale benefit the cost of PAD

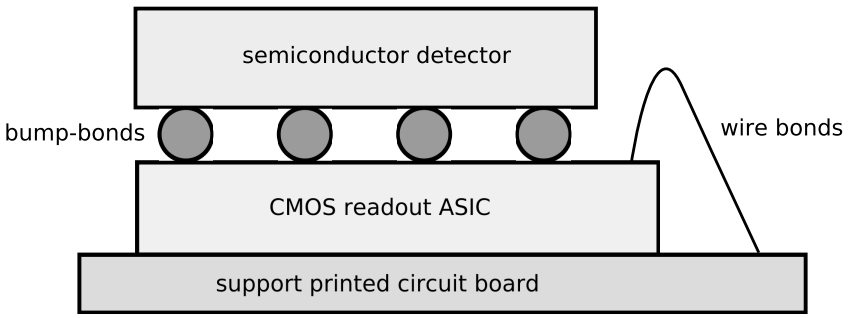
designs. Since PADs are based on direct x-ray detection in semiconductors the intrinsic noise, collection speed, and spatial resolution are excellent. The flexibility of the pixel processing electronics is immense as hundreds of transistors may fit into the area of an ASIC pixel.

Two primary approaches for the PAD readout ASIC have been implemented. In one approach individual x-rays are counted; sufficient charge is deposited per x-ray (~ 0.5 fC) that the voltage pulse induced at the readout pixel by each x-ray may be detected and counted. In a contrasting architecture the x-ray induced charge is integrated during the exposure time and the pixel voltage is digitized at exposure end. The next sections present current implementations, consider strengths and weaknesses, and explore the time resolution of each approach.

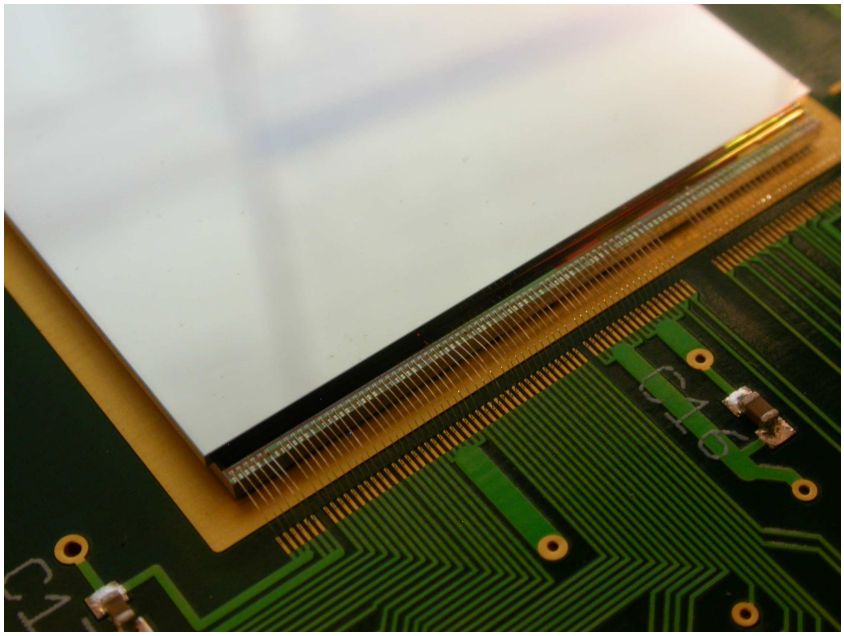
1.3.4.1 Photon counting

A generalized schematic of a photon counting pixel is shown in Figure 1.5. The charge pulse from an x-ray is amplified with a gain typically around $10\,\mathrm{mV/ke^-}$ [45]. The output of a shaper, which limits the bandwidth of the pre-amplifier, is monitored by a comparator. When the shaper output exceeds a threshold level the comparator triggers and the in-pixel counter is incremented. At the end of an exposure the pixel output is the digital number stored in the counter.

Photon counting is a low-noise approach that is insensitive to thermally generated current from the detector layer (dark current). Further, dual discrimination may be utilized to limit detection to a window of x-ray energies. Photon counting is complicated for x-rays that convert in areas of the detector where charge diffusion causes a division of the signal among multiple pixels in the readout ASIC (charge sharing). The Medipix collaboration has developed a pro-



(a)



(b)

Figure 1.4: (a) A drawing showing the hybrid configuration of a PAD. The semiconductor detector layer is divided into pixels, each of which are connected via a bump-bond to a pixel in the CMOS readout chip. The CMOS readout chip processes the charge created in the detector layer and outputs electrical signals (shown by a wire-bond at right) to support electronics for data storage. (b) A photograph of a PAD connected to a support printed circuit board. The imaging area for this device is an 185×194 array of pixels that covers 20.3×21.3 mm^2 (photograph by Mark W. Tate).

totype photon counting readout ASIC with neighboring pixel communication to mitigate the counting ambiguity induced by charge sharing [46]. Photon counting PADs have a detection rate limit of about 10 million x-rays per pixel per

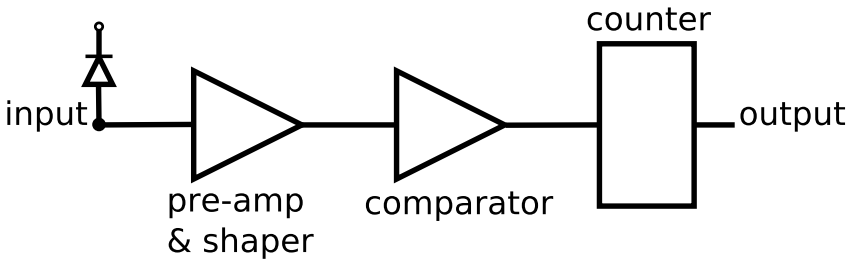


Figure 1.5: A schematic of a photon counting PAD showing the essential electronic elements. Charge from a semiconductor detector enters at the left and is processed by a pre-amplifier and shaper. A comparator monitors the shaper output for levels above a specified threshold and, when triggered, increments an in-pixel counter. At the end of an exposure the pixel output is the value stored in the counter.

second due to the time required to process each charge pulse.

The PILATUS is a single photon counting PAD designed primarily for protein crystallography [47]. The in-pixel counter may be disabled by an external signal. The counter gate has been used to isolate single-bunches from the APS synchrotron ring [18]. Photon counting, however, enforced a count-rate maximum of one x-ray per-pixel per-bunch since the pre-amplifier and shaper required a recovery time of 125 ns after detection of an x-ray before detection of another [18]. Further, due to Poisson fluctuations in the x-ray signal the per-pixel per-bunch signal must be held to an average of less than 1 x-ray (otherwise a significant number of bunches would produce multiple x-rays per pixel which would be incorrectly recorded). For example, the probability of multiple arrivals in a single bunch exceeds 10% at a mean per-bunch per-pixel photon level of 0.55. The accuracy of measurement of the intensity of an x-ray feature is ultimately limited by Poisson statistics to $\sqrt{N}/N$ for the detection of N x-rays, which dramatically limits the accuracy possible with photon counting detectors in single or few bunch experiments.

1.3.4.2 Analog integrating

Analog integrating PADs have measured fluxes that approached 10^{12} x-rays/pixel/second which suprasses the count-rates reached by counting PADs [48]. Figure 1.6 displays a simplified schematic of an integrating PAD pixel. X-ray induced charge is integrated across the feedback capacitor, C_{INT}, of

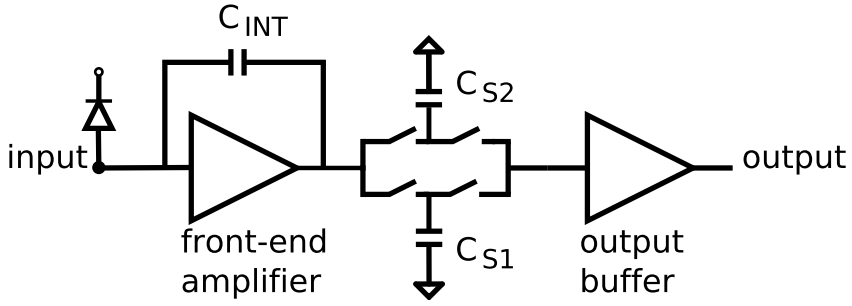


Figure 1.6: A schematic that shows the basics of an analog integrating PAD. X-ray induced charge is integrated across the feedback capacitance C_{INT} of the front-end amplifier. At the end of an exposure the output voltage is stored on an in-pixel capacitor for later readout by the output buffer.

the front-end amplifier. At the end of an exposure the voltage at the front-end amplifier output is stored on an analog memory element. The example pixel of Figure 1.6 shows two in-pixel storage elements, C_{S1} and C_{S2}. In-pixel memory has allowed for rapid acquisition of successive images at rates that far exceed the rate of readout and digitization. The capacity per storage element is set by the voltage range of the pixel electronics and the gain of the front-end charge amplifier. This dissertation will show that capacities of 4,000 x-rays or more are feasible with noise levels around 1 x-ray. Integrating PAD readout pixels collect all charge from the detector layer. Because of this, they do not encounter systematic problems when charge is shared between multiple pixels. Since the signal is output in analog form noise is associated with detector readout (read-noise). Analog integrating PADs do not limit the front-end amplifier bandwidth

in the way photon counting PADs do and, as such, are sensitive to detector dark current.

Analog PADs are a focus of the detector group at Cornell University. The 100×92 detector featured eight in-pixel storage elements and speed for microsecond imaging experiments [48]. This prototype detector has been applied to microsecond radiography and diffraction experiments [20, 49]. Further work at Cornell has extended the dynamic range of the analog integrating approach by implementation of in-pixel near-overflow detection and charge removal. Each removal increments an in-pixel digital counter. For this mixed analog and digital approach the pixel output is the combination of the coarse digital counter value and the fine resolution analog value (named 'mixed-mode PAD' or MM-PAD) [50]. The large hit-rate capabilities of an analog PAD along with in-pixel analog-to-digital conversion have been used by the Cornell group to develop a low-noise high instantaneous flux-rate x-ray detector. This detector is designed for use at the linac coherent light source (LCLS) under development at Stanford where the x-ray signal arrives in femtoseconds (named 'LCLS PAD') [51].

Work on fast analog sampling detectors away from Cornell include that of Kleinfelder and co-workers who have developed a one-dimensional detector array of 150 pixels with 150-deep analog storage elements [52]. This work, targeted most specifically to proton radiography, reported a sampling speed of 100 MHz for optical signals. Their other developments include a two-dimensional array of in-situ storage pixels. A bandwidth of up to 7 MHz for electrical test signals was reported but optical detection was not presented [53]. A consortium of the Universities of Bonn and Hamburg, Deutsches Elektronen Synchrotron (DESY), and Paul Scherrer Institut (PSI) are currently developing an adaptive gain analog integrating PAD for use at the European x-ray free elec-

tron laser (XFEL) [54]. Experiments at the European XFEL, like the LCLS, will produce pixel flux-rates that exceed the capabilities of photon counting detectors.

1.3.5 Avalanche photodiodes and streak cameras

Two other x-ray detectors, designed primarily for fast response, deserve discussion. Avalanche photo diodes rely upon high-field carrier multiplication in a silicon detector to increase signal currents to levels detectable by fast, conventional electronics. Streak cameras access time resolutions of < 1 ps making possible the study of dynamics within a single x-ray pulse.

1.3.5.1 Avalanche photodiodes

The drift field within avalanche photodiodes (APDs) provides sufficient velocity to charge carriers to induce amplification via impact ionization. Avalanche devices for x-ray detection are most commonly operated in a linear amplification regime with a signal gain of 10-100 [55]. Charge carrier amplification makes possible the detection of single x-ray pulses by cabled high-speed electronics. The APD signal is processed by a high-bandwidth ($\sim$GHz) voltage amplifier which is coupled to a discriminator and counter. External electronics that have been used are capable of dead-times around 5 ns and counting rates that approach $10^8\,\mathrm{s}^{-1}$ [55]. These setups produce a single bunch resolving detector, with continuous data capture, that is limited to one pixel and one count per bunch.

Work at the APS has used an APD without x-ray pulse counting to increase the maximum number of x-rays detected per bunch. In this configuration the amplified APD signal is captured by a 500 MHz oscilloscope with 1-2 ns tem-

poral resolution over a record-length of 10 μs [56]. This analog APD approach remained linear for signals up to 500 x-rays per bunch.

1.3.5.2 Streak cameras

X-ray streak cameras use high-speed electron optics to encode temporal dispersion into a spatial distribution. X-rays incident onto a photocathode[6] eject electrons that are accelerated by a constant extraction field of around 100 kV/cm. Once accelerated the electrons pass between parallel deflection plates to which a swept potential, triggered by a photoconductive switch, is applied. Deflection plates have produced sweep speeds of 2×10^8 m/s, which implies a deflection of 200 μm for a 1 ps temporal dispersion [58]. After deflection the electrons are often amplified by a micro-channel-plate before being converted to light by a phosphor. An area CCD detector records the phosphor signal and encodes spatial information along one dimension and temporal information along the other. Streak cameras have been reported with 233 fs time resolution and 10 μm spatial resolution [57]. The efficiency and temporal resolution of streak camera photocathodes is inherently coupled. Most streak cameras trade x-ray stopping efficiency for time resolution. The low efficiency has forced operation in accumulation mode – multiple x-ray pulses are measured before CCD readout. Streak cameras are the most prevalent tool for studies of intra-bunch dynamics. However, one-dimensional spatial resolution and low x-ray efficiency, which hinders single-shot applications, limits the range of x-ray experiments appropriate for streak cameras.

[6] Photocathode materials include Au, CsI, and Ag [57].

1.4 Conclusion

Direct x-ray detection in silicon has excellent efficiency and is sufficiently fast for high-speed experiments. Avalanche photo diodes have been used for single-bunch imaging but are generally only single pixel devices. PADs are area detectors with a CMOS readout chip coupled to a direct detection layer. Photon counting PADs have been shown to gate in-pixel counting with timing sufficient for single-bunch imaging, yet the count-rate of 1 x-ray per pixel per bunch limits the accuracy of a measurement. CCDs do not have count-rate constraints but time resolution is set by the time to read a frame. Analog integrating PADs with in-pixel storage are capable of reaching accuracies in single-bunch experiments far beyond photon counting devices due to a much larger count-rate limit. In this dissertation, integrating PADs are shown to capture successive frames at rates commensurate with single-bunch imaging.

1.5 Dissertation organization

Chapter one motivates the development of an area pixel array x-ray detector capable of isolating single bunches from the synchrotron. Chapter two presents time-resolved x-ray experiments done at the Cornell High Energy Synchrotron Source (CHESS) and the Advanced Photon Source on reactive metal foils using a pixel array detector. These studies provide insight into solid-state phase transformation and growth at high heating rates and large concentration gradients and also motivate high-speed x-ray detector development. Chapter three presents the tools needed for design of CMOS electronics for a detector sufficiently fast to resolve single synchrotron bunches. After the tools are explained a prototype chip is discussed and test results from the chip are presented. Suc-

cessful testing of the first prototype chip encouraged the work of chapter four which was to design a full camera system, complete with a hybridized detector layer and FPGA based control and acquisition. In chapter 5 experimental testing of the camera is presented, which includes high-speed pulsed laser tests and experiments at CHESS.

This dissertation work furthered the development of analog PADs with in-pixel storage designed by the Cornell detector team. The innovative contributions include lock-in like capabilities, experimental demonstration of time resolution sufficient to isolate successive x-ray bunches, and development of robust control electronics with flexible field-programmable-gate-array (FPGA) code to allow for utilization of the multitude of imaging modes offered by the pixel electronics.

CHAPTER 2

STUDIES OF TRANSIENT PHASE TRANSFORMATIONS USING A PIXEL ARRAY DETECTOR

2.1 Introduction

This chapter presents time-resolved x-ray diffraction experiments that used a PAD and high-flux x-ray optics to study phase transformations at heating rates around $10^6\,\mathrm{K\,s^{-1}}$. These experiments motivate development of advanced x-ray detectors. Two methods to focus x-rays for maximum flux into spots of $60\,\mu$m or less are presented. Lessons are drawn from this experimental work that will be applied to the detector development presented later in this dissertation. Since many of the results have been published[1], this chapter shifts the focus toward a few methods in detail, detector issues and developments specific to this experiment, and unpublished results from an experiment at the Advanced Photon Source. This work was highly collaborative. The acknowledgement section contains a list of all who participated. Dr. Jonathan Trenkle, from Johns Hopkins University, deserves particular recognition.

2.1.1 Reactive multilayer foils

Reactive multilayer foils (RMLFs) are alternating nanoscale layers of materials with a negative heat of mixing sufficient to sustain a self-propagating reaction. A schematic displaying regions of reacted foil and un-reacted foil, as well as directions of thermal diffusion, atomic diffusion, and reaction front propagation is shown in Figure 2.1. After an activation event the reaction self-propagates,

[1]This work has been published in Applied Physics Letters [49] and in the Journal of Applied Physics [59]. It has also been presented at the JANNAF 2008 symposium, and at the 2007 and 2008 Materials Research Society (MRS) Fall Meetings.

as mixing releases heat which drives atomic diffusion to subsequently produce more mixing. The reaction front temperature may exceed 1300 K in less than 10 μs for a heating rate of 10^8 K s^{-1} [60]. The foils we studied were on the order of tens of microns thick and were composed of sputter-deposited layers around 10-100 nanometers thick.

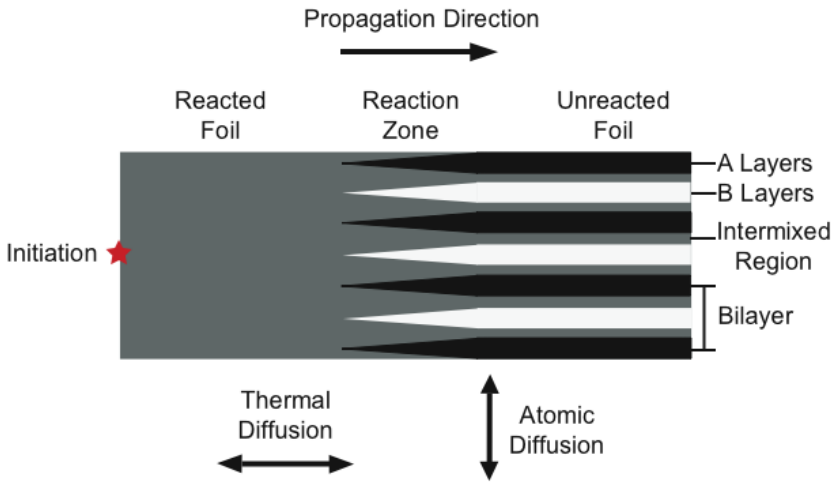


Figure 2.1: Schematic of a reactive multilayer foil consisting of layers 'A' shown in black and layers 'B' shown in white with a reaction propagating to the right. From reference [61].

RMLFs have been applied as a localized heat source for joining sensitive components [62]. For example, they have been used to weld metallic glasses. Metallic glasses have unique mechanical properties; their larger elastic strain limit than conventional crystalline materials has been utilized to make high performance springs [63]. However, metallic glasses are difficult to join because cooling rates must be sufficiently rapid to prevent crystallization [64, 61]. A RMLF ignited between two pieces of metallic glass may join the parts without inducing crystallization since the heat released is minimal and localized.

The industrial applications of RMLFs provide motivation for the study of their phase transformations. The progression of the microstructure during unabated reactions of RMLFs is relatively unknown but will determine the prop-

erties of the reacted film. A second motivator is that RMLFs provide a system to study the science of phase transformations and grain growth in thin films. Integrated circuit fabrication, x-ray optics, and protective coatings are all dependent upon thin film technologies [65]. The growth and nucleation of crystalline phases in thin films has a direct impact on performance parameters [65]. For example, the resistivity of copper interconnects within integrated circuits depends upon grain size [66]. Relevant studies of thin films are lacking and knowledge of nucleation and growth of intermetallic phases from bulk materials cannot simply be extrapolated to thin films. This is because thin films have higher concentration gradients and more significant interfacial energies than bulk samples [67]. The studies presented here also differ dramatically from others in heating rate. At the high heating rates studied in this work, the time required for diffusion and nucleation is limited. *In situ* x-ray studies of RMLFs advance the understanding of phase transformations away from equilibrium: at high-heating rates, at nanoscale dimensions of thin films, and with large concentration gradients.

2.2 Experimental methods

2.2.1 Powder diffraction

Solid metals are most often composed of many crystallites, of varying sizes and arbitrary orientations, called grains. Due to the random orientations, diffraction from many grains produces scattering in a cone symmetric about the azimuth (termed powder diffraction). The scattering angle is related to the momentum transfer imparted to the incident x-rays by,

$$q = \frac{4\pi}{\lambda} \sin\theta, \tag{2.1}$$

where q is the momentum transfer, λ is the x-ray wavelength, and θ is half of the scattering angle. The momentum transfer that satisfies Bragg's law may be related to the scattering plane spacing, d, as $q = (2\pi)/d$. The scattering geometry is shown in Figure 2.2.

2.2.1.1 Anticipated scattering intensity

Preparation for time-resolved experiments require calculations of the fraction of the incident x-ray signal scattered onto the detector. The scattered power from a crystalline plane in a powder sample is given, in cgs units, as [68],

$$P_{scat} = I_0 \overbrace{\left(\frac{e^4}{m_e^2 c^4}\right)}^{\text{e}^- \text{ scat. len. sq.}} \frac{V\lambda m F_T^2}{4\upsilon^2} \overbrace{\left(\frac{1+\cos(2\theta)^2}{2\sin(\theta)}\right)}^{\text{LP}}. \tag{2.2}$$

I_0 is the incident x-ray intensity, e and m_e are the charge and mass of an electron, respectively, c is the speed of light, and the expression $e^4/(m_e^2 c^4)$ is the square of the electron scattering length. V is the volume of sample probed, m is the multiplicity of the crystalline plane, F_T is the structure factor of the plane, and υ is the unit-cell volume. LP indicates the Lorentz-polarization factor: the Lorentz factor, $1/\sin\theta$, accounts for the fraction of crystallites with correct orientations to satisfy the Bragg condition, and the polarization factor, $(1+\cos(2\theta)^2)/2$, accounts for the dependence of the scattered intensity on the polarization of the incident beam. Equation 2.2 has assumed an unpolarized incident beam.

For this specific experimental configuration, equation 2.2 must be modified to a more appropriate form. First, the equation is simplified, by relating the incident x-ray intensity to the incident x-ray power, P_0, and the cross-sectional area of the sample probed, A, as $I_0 = P_0/A$. The sample volume probed is written as the thickness, L, multiplied by the cross-sectional area to give, $V = AL$. Second, synchrotron sources produce radiation polarized parallel to the plane of

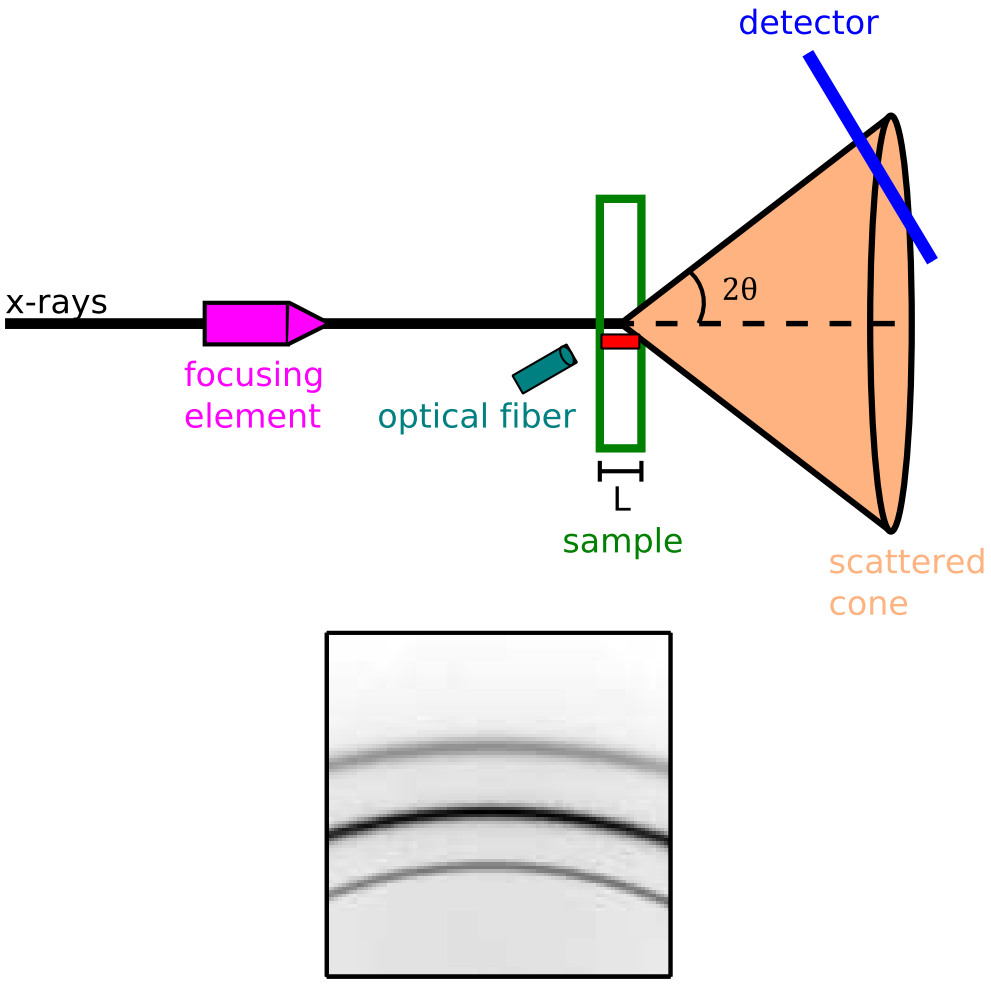


Figure 2.2: Top, a schematic of the RMLF experimental configuration. X-rays that entered from the left were focused and interacted with the sample (of thickness L). An optical fiber detected light from the propagating reaction front (shown in red) and triggered the x-ray detector. X-rays scattered at an angle 2θ into a cone symmetric about the incident x-ray beam are shown. The detector (blue) was positioned normal to the diffracted beams of interest and captured a partial section of the cone. At the bottom is an example diffraction pattern with rings from three separate crystalline planes (dark represents higher x-ray intensity).

the electron orbit such that, for scattering in the vertical plane (the case of these experiments), the polarization factor is one [69]. Last, x-ray absorption by the sample must be considered. The non-symmetric transmission geometry of our

experiments complicates the absorption calculation. Absorption is represented by the term $Ab(\theta)$. The result is the power scattered, P_{scat}, into a powder ring,

$$P_{scat} = P_0 \overbrace{\left(\frac{e^4}{m^2c^4}\right)}^{\text{e}^- \text{ scat. len. sq.}} \frac{L\lambda m F_T^2}{4v^2} \overbrace{\left(\frac{1}{\sin(\theta)}\right)}^{\text{Lorentz}} Ab(\theta). \tag{2.3}$$

2.2.1.2 Absorption with oblique exit

Two options exist for the geometry of crystal x-ray diffraction experiments: reflection (Bragg) or transmission (Laue) [69]. In reflection (transmission) geometry the incident x-rays enter the sample through the same (opposite) surface as the exiting diffracted x-rays that are detected. A reflection configuration is symmetric if the surface normal is parallel to the diffracting crystalline planes. A symmetric transmission geometry has the surface normal perpendicular to the diffracting planes. These geometries are presented in Figure 2.3. The small physical size of the detector used in this experiment forced a sample to detector distance on the order of a few centimeters to cover the desired range of scattering angles. A small separation between the sample and detector excluded a reflection geometry since the PAD housing would have blocked the path of the incident beam to the sample. The RMLF experiments used a non-symmetric transmission geometry, which is important to recall when texture effects are considered.[2]

A transmission geometry requires careful selection of beam energy and sample thickness. If the sample is too thin, few x-rays diffract; if the sample is overly thick most x-rays that diffract are attenuated by the sample on the way to the detector. An optimal beam-energy and sample thickness can be found that

[2] "Texture" refers to preferred orientation of the sample grains. Details of sample fabrication may result in a tendency for grains to align with the sample surface. In a non-symmetric Laue geometry preferential crystallite alignment with respect to the sample surface depletes the number of grains that satisfy the diffraction condition.

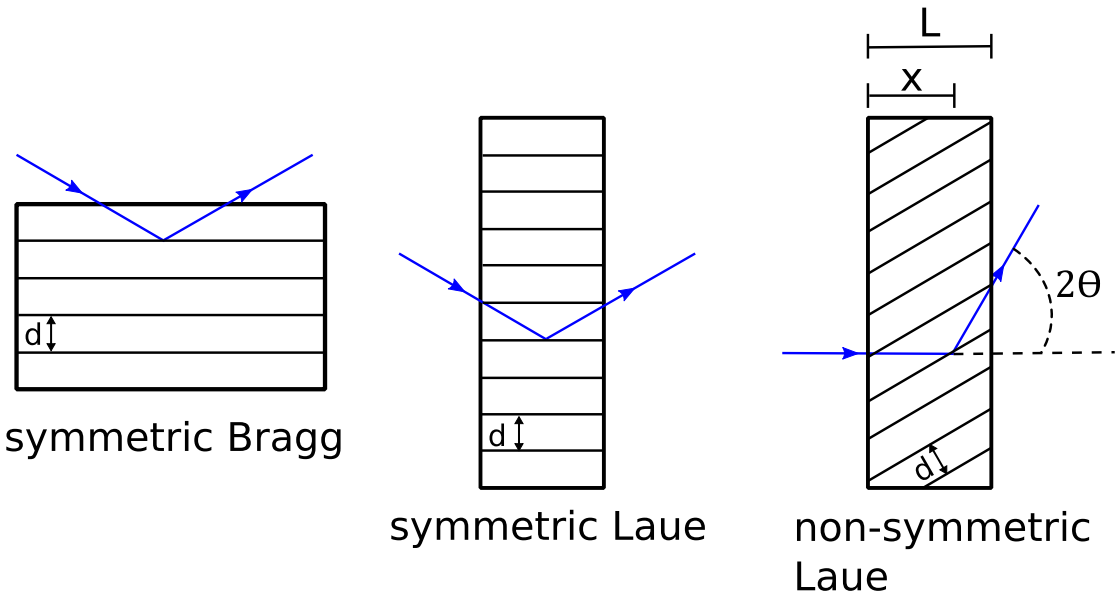


Figure 2.3: Possible crystal diffraction geometries, adapted from reference [69]. Incident and diffracted x-rays are indicated in blue. Our experiments were configured in non-symmetric Laue geometry.

maximizes the detected diffraction.

The probability of absorption of a scattered x-ray depends upon the scattering angle and the location along the sample thickness that the scattering occurs. With reference to the right-most geometry shown in Figure 2.3, in the kinematic approximation, a probability distribution for the location of scattering is found as:

$$P(x) = \int_0^L R\frac{e^{-x/\mu}}{L}dx, \tag{2.4}$$

where μ is the absorption length of the sample and R is a constant to normalize the probability distribution to one. The probability of absorption if diffraction occurs at point x and at an angle 2θ is given as,

$$A(x) = e^{-x/\mu}e^{-(L-x)/(\mu\cos 2\theta)}, \tag{2.5}$$

since $(L-x)/\cos 2\theta$ is the length out of the sample after a ray is scattered at an angle 2θ at point x. The fraction of incident x-rays absorbed as a function of

scattering angle is then found as,

$$Ab(\theta) = \int_0^L A(x)P(x)dx = \frac{1}{\mu}\frac{e^{-L/(\mu\cos 2\theta)}}{(1-e^{-L/\mu})}\int_0^L e^{-x(2\cos 2\theta - 1)/(\mu\cos 2\theta)}dx. \tag{2.6}$$

The result of the integration is:

$$Ab(\theta) = \left(\frac{1}{1-e^{-L/\mu}}\right)\left(\frac{\cos 2\theta}{2\cos 2\theta - 1}\right)(e^{-L/(\mu\cos 2\theta)} - e^{-2L/\mu}). \tag{2.7}$$

At $\theta = 0$ the absorption factor is reduced to $Ab(\theta = 0) = e^{-L/\mu}$ as expected. The dependence of absorption on scattering angle is especially important for experiments that require a sample thicker than a few absorption lengths. The maximum of $Ab(\theta)L$ with respect to L gives the sample thickness for optimal scattering intensity. Once the experimental results are presented the above expressions will be used to compare the anticipated and measured signals.

In the RMLF experiments samples consist of alternating layers with different absorption lengths (μ_1, μ_2) and thicknesses (L_1, L_2 where $L = L_1 + L_2$). The total absorption can be written as,

$$e^{-L_1/\mu_1}e^{-L_2/\mu_2} = e^{(L_1+L_2)/\mu_{tot}}, \tag{2.8}$$

where the composite absorption length is:

$$\mu_{tot} = \frac{(L_1+L_2)(\mu_1\mu_2)}{L_1\mu_2 + L_2\mu_1}. \tag{2.9}$$

2.2.2 Multiple capture microsecond framing PAD

The width in the direction parallel to propagation and velocity of the reaction front determine the temporal resolution required of the x-ray detector. The front has been measured to be around 100 μm in width. Therefore, fronts moving at 1-10 m/s pass a fixed point in 10-100 μs, which sets the required time resolution.

To achieve this time resolution an analog integrating PAD was used. A

schematic of the CMOS pixel is shown in Figure 2.4, which works as follows: the photo-charge produces a voltage change at the output of the input stage which is stored on one of eight analog storage elements (C_{S1}-C_{S8}). The analog storage elements allow the capture of eight successive frames with microsecond temporal spacing before a slower, raster-scan readout to an off-chip analog-to-digital converter. The capture of eight time sequences from each foil was valuable for confirmation of data consistency.

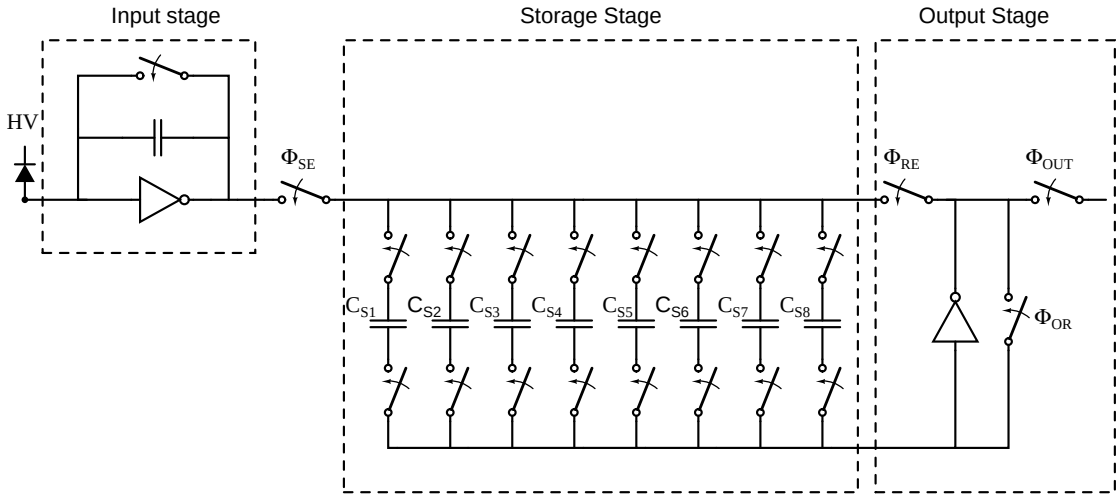


Figure 2.4: Schematic of a pixel within the CMOS readout chip of the microsecond framing PAD used for transient phase transformation studies.

This PAD consisted of a 100×92 array of $150\,\mu$m square pixels (1.50×1.38 cm overall). The detector was constructed as a hybrid of a $300\,\mu$m thick pixellated, fully-depleted silicon PiN diode layer manufactured by SINTEF. The CMOS readout chip was designed in a Hewlett-Packard $1.2\,\mu$m process. In terms of 8.9 keV x-rays, the full-well capacity has been measured to be 17,000 and the RMS pixel read-noise to be 2.5 [48].

2.2.3 Focusing elements

The x-ray spot on the sample must match or be smaller than the size of the reaction front, so that temporal dynamics are not smeared. Focusing optics were used to achieve the desired x-ray spot size and maximize the flux to the sample. Time resolved x-ray experiments with PADs often benefit from focused x-ray spots. For future reference, two methods that were used to focus x-rays are discussed: single-bounce monocapillaries and Kirkpatrick-Baez mirrors. Both optics rely upon total external reflection. The index of refraction for x-rays in materials is less than the index of vacuum, so that at grazing incidence Snell's law is satisfied without a transmitted beam and all incident power is reflected. The critical angle, below which the beam is entirely reflected, is given as $\theta_c \cong \sqrt{2\delta}$, with the index of refraction represented as $n = 1 - \delta + i\beta$ [70, 69].

2.2.3.1 Single-bounce monocapillaries

A single-bounce monocapillary is a hollow glass tube pulled into a highly eccentric ellipse. X-rays reflect once, with > 95% efficiency, from the inside of the capillary walls and are concentrated to a foci of the ellipse [71]. Monocapillaries designed and tested at CHESS have energy independent focusing characteristics, reasonable working distances of a few centimeters, produced divergences of 2-8 mrad, and focused x-rays to spots of 10-20 μm FWHM [71].

2.2.3.2 Kirkpatrick-Baez mirrors

Kirkpatrick-Baez (KB) mirrors also rely upon elliptically shaped reflecting surfaces to focus x-rays. Horizontal and vertical focusing are done by separate bounces off of two orthogonal mirrors. The mirrors consist of a metallic coated (often platinum or rhodium) silicon substrate, curved to the required elliptical

figure by motors. Since the mirrors are sensitive to damage by radiation they are generally housed in an inert atmosphere, which limits the minimum focal length. KB mirrors have better slope and profile errors than monocapillaries do, which makes them more suitable for exploiting the low-emittance of third generation sources [72]. KB mirrors have reached spot-sizes as small as 100 nm FWHM [70].

2.2.3.3 Focusing discussion and comparison

KB mirrors have excelled at the production of micron sized x-ray spots. But, as will be seen in the experiments done at the APS, a powder diffraction experiment requires a large enough spot to ensure that a sufficient number of crystallites are sampled by the x-ray beam. KB mirrors require an inert atmosphere and have an adjustable figure, which makes their configuration more complex than a monocapillary. CHESS and the APS have collaborated on a comparison of KB mirrors and monocapillaries at the APS 18ID beamline with interesting results [72]. The monocapillaries worked well with upstream focusing whereas the KB mirrors did not. Because of the difference in accepted incoming flux the monocapillary produced ten-times more flux into a similar sized spot than the KB mirror setup [70].

2.3 Experiments at CHESS A2

2.3.1 Experimental setup

Sagittal focusing multilayer optics of W/B_4C with 28 Å d-spacing were used to focus the X-ray beam from a 49-pole wiggler [73]. The energy bandpass of the optics was $\Delta E/E = 1.9\%$ and the energy was tuned to 8.2 keV to avoid nickel flu-

orescence and to maximize detector efficiency (98 % at selected energy). The flux was measured to be 8.9×10^{13} x-rays/mm^2/s using a helium filled ion-chamber at a ring current of 198 mA at 5.3 GeV.

Monocapillary Peb605 developed at CHESS with 8 mrad divergence, 455 flux gain, and an entrance inner-diameter of 827 μm was used to further focus the x-ray beam to a 60 μm spot [71] ('focusing element' in Figure 2.2). The monocapillary was created by the group of Don Bilderback and installed by Sterling Cornaby. This specific monocapillary was selected because it offered the largest flux gain. The capillary focal-length of 55 mm allowed reasonable access to the sample. After the capillary, a flux of 1×10^{13} x-rays/mm^2/s was measured at the focal-spot. The increased beam divergence from the monocapillary did not overly degrade the reciprocal space resolution due to the wide x-ray energy bandpass and large angular size of the detector pixels. A quantitative comparison of the reciprocal space resolution limits in the reactive foil experiment imparted by the monocapillary divergence, the detector resolution, and the x-ray energy spread is discussed in the dissertation of Sterling Cornaby [70]. The figure of merit for this experiment was simply the number of photons in a spot small enough to match the size of the reaction front.

To cover a large range of scattering angles the detector was centered on diffracted beams of interest such that only partial diffraction rings were captured. The detector was $\approx$ 22 mm from the sample and inclined $\approx 45°$. With this orientation scattering vectors from q = 1.86 to 4.34 $\mathring{A}^{-1}$ were observed and $\sim$15 % of the circumference of the powder rings were captured (see Figure 2.2). A 13×25 mm section of reactive foil was clamped between two sheets of stainless steel that were 0.75 mm thick, 75 mm wide, and 20 mm tall ('sample' in Figure 2.2). The reaction was initiated by a spark produced by a voltage applied

to a sharp tip. The needle tip was driven to proximity of the foil via an electromagnet. The reaction propagated along the long direction of the foil.

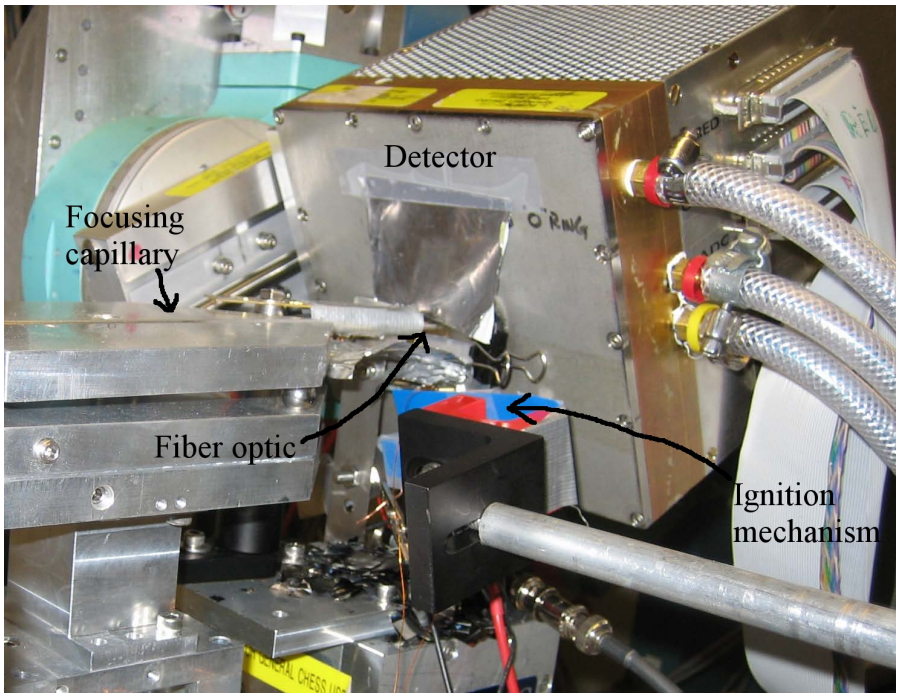


Figure 2.5: A labeled photograph of the RMLF experimental setup at CHESS A2 hutch. The x-rays enter from the left-side, are focused by the capillary, and interact with the foil samples. The samples are not clearly visible but are near the arrow that points toward the fiber optic.

An optical fiber, which had a 200 μm diameter and an 8.5° collection angle, was placed 1.5 cm from the foil and detected the arrival of the reaction just before the front crossed the x-ray beam. The optical fiber was connected to an InGaAs photodetector (700 - 1800 nm detectable wavelength range), which triggered a pulse height analyzer/digital delay generator (Stanford Research Systems, Sunnyvale, CA, model DSG 535). The delay generator controlled the time between detection of the reaction front and start of the PAD exposure.

The sample temperature was measured using a ratio pyrometer based upon the design in reference [74]. A ratio pyrometer extracts temperature from the

intensity of light emitted by a source at two wavelengths, λ_1 and λ_2. After calibration with a black-body source, the ratio of the intensities can be directly related to the sample temperature independent of spot size, detector responsivity, signal amplification, etc. In our experiments the emission from the sample was gathered by a fiber-optic, split by a dichroic mirror, and filtered to wavelengths of $\lambda_1 = 1600\,\text{nm}$ and $\lambda_2 = 1395\,\text{nm}$ before detection. The original experimental design was to trigger the PAD using the amplified signal of one of the filtered wavelengths from the ratio pyrometer. However, the intensity proved insufficient for reliable triggering, such that one of the filters had to be removed and temperature measurements at the beamline were abandoned. In a later set of experiments the CHESS beamline setup was reproduced by Jonathan Trenkle and the temperature-time profiles (black curve in Figure 2.6) of the RMLFs were measured.

2.3.2 Results

An example of the information obtained in the RMFL experiments is shown for the Al_3Ni_2 foils in Figure 2.6. The top (a) shows diffraction patterns acquired before, during, and after passage of the reaction front. The bottom (b) shows the integrated peak area (proportional to the volume fraction of the phase) of all phases found versus time. In all, three sample compositions were studied at CHESS with the following results.

- **Al_3Ni_2**: These foils initially formed an AlNi intermetallic and an Al-rich amorphous phase. During cooling Al_3Ni_2 formed from the AlNi and liquid. The phase progressions found were different than experiments at slower heating rates which detected a metastable Al_9Ni_2 phase and did not observe an amorphous phase [49].

- **AlNi**: AlNi intermetallic and an Al liquid formed first. During cooling the AlNi phase grew as the amorphous phase was consumed. Again, the phase progression differed from slow-heating which has shown a sequence with three intermediate metastable phases [59].
- **$Zr_{55}Ni_{45}$**: ZrNi and an amorphous phase formed first. During cooling Zr_2Ni formed and ZrNi remained. In this case the foil temperature did not exceed the melting temperature of either of the elemental constituents but an amorphous phase was detected. Most likely, a solid-state amporphization reaction occurred as Ni diffused into Zr [59].

The differences found in the phase progression between freely propagating reaction fronts studied here and foils heated at slower rates are important to both the fundamental material science of thin-film reactions and the application of thin-film materials. When applications are considered, the relevant material properties of the final reaction product depend upon both the compounds formed and details of the microstructure. The phase progression is important to understand since it will influence the final microstructure of the reaction end product. Cooling-rate has been used as an adjustable parameter to dictate materials properties during solidification of metallic glasses [61] or the solvent within protein crystals [75]. In a similar fashion, directed tuning of the heating-rate to achieve specific properties of final product may be feasible. Identification of the phase progression at high-heating rates would help tuning of the heating-rate for a desired property. Finally, applications may require knowledge of particular material properties of the actual reaction front, which are elucidated by identification of the phases present as the reaction proceeds.

Scientifically, predictions of phase formation remain elusive for reactions at interfaces and when the time for formation of nuclei is limited [65]. Many

theoretical works have attempted to explain the kinetics of thin-film reactions [76, 67]. Experimental verifications with thin-film samples at rapid-heating rates are valuable for these theoretical models.

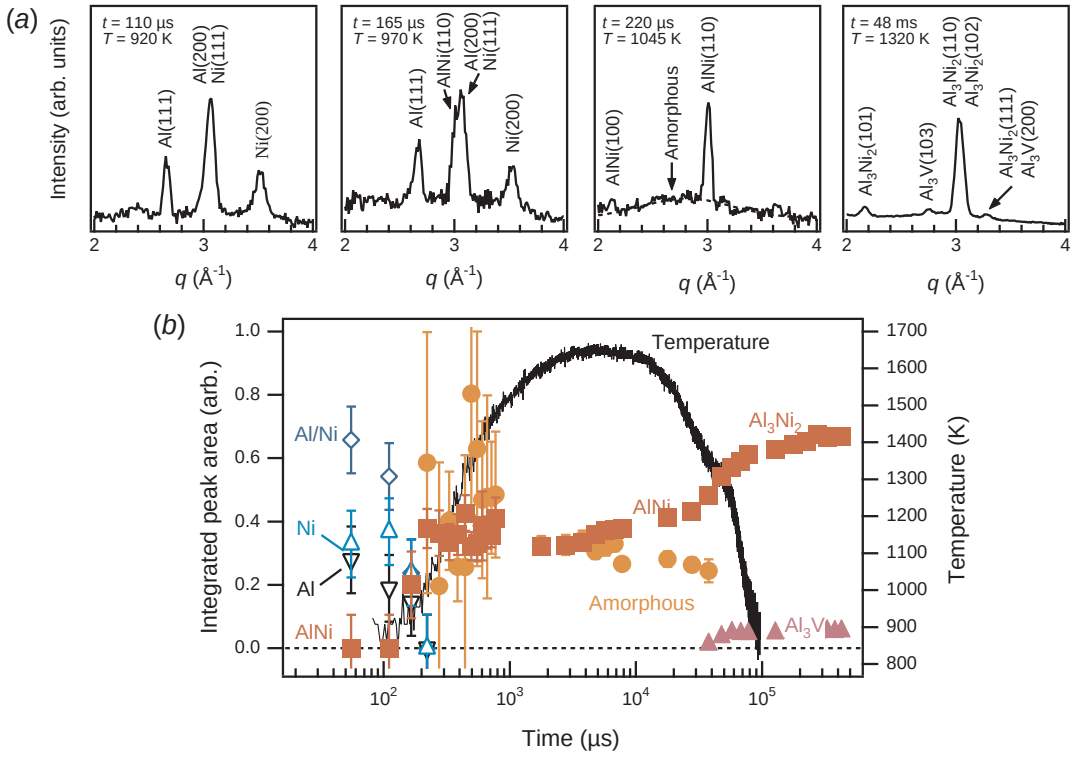


Figure 2.6: (a)Diffraction patterns recorded at various times t during the reaction and through cooling. Note that the reaction front arrives at the x-ray beam at $t = 180 \pm 20\,\mu$s, so that the first pattern is from the unreacted foil. (b) Normalized integrated peak area and reaction temperature. Because two overlapping peaks from Al_3Ni_2 cannot be resolved from the AlNi(110) peak over the interval when Al_3Ni_2 forms (t=30-50 ms) the peaks from both phases are represented by a single symbol. Analysis by Jonathan Trenkle. Reprinted with permission from J.C. Trenkle, L.J. Koerner, M.W. Tate, S.M. Gruner, T.P. Weihs and T.C. Hufnagel, *Applied Physics Letters*, 93, 081903, 2008. Copyright 2008, American Institute of Physics.

2.3.2.1 Comparison of anticipated and experimental signal

Table 2.1 compares calculated and measured scattering intensities. The calculations exceed the measured values by $\approx \times 25$; this is not surprising. Many unaccounted for effects would reduce the intensity measured from that calculated: sample texture, over-estimation of the incident intensity, polarization factor less than one, and sample heating due to the incident x-rays. The importance of this calculation is to reinforce that it is possible to estimate the minimum achievable time resolution given the incident x-ray intensity, sample scattering power, and the noise of the detector.

Table 2.1: Calculated scattering intensities using equation 2.3 and measured scattering intensities for the Al_3Ni_2 foils studied at CHESS A2. d is the diffracting plane lattice parameter. f is the atomic scattering factor (for face-centered cubic (fcc) Bravais lattice $F_T = 4f$ with unmixed hkl). Abs is the absorption calculated from equation 2.7. $Frac_{Ring}$ is the fraction of the Debye ring measured by the detector. Debye is the intensity reduction anticipated due to thermal vibrations at a sample temperature of 293 K [69]. Other constants required: λ=1.51 Å, L_{Al} = 21 μm, L_{Ni} = 9 μm, μ_{Al} = 83.5 μm, μ_{Ni} = 25.4 μm, $I_0 = 1 \times 10^{13}$. Ni(111) and Al(200) were not separately resolvable so the measured intensity reported is the sum of the two peaks.

Material	hkl	m	d (Å)	θ	$\sin(\theta)/\lambda$	f	Abs	$Frac_{Ring}$	Debye	I_{Calc}	I_{meas}
Al (fcc)	111	8	2.34	18.84	0.21	9.03	0.5	0.16	0.97	8.38×10^8	3.45×10^7
Ni (fcc)	200	6	1.76	25.37	0.28	19.42	0.45	0.12	0.97	1.49×10^9	4.25×10^7
Ni (fcc)	111	8	2.03	21.79	0.25	20.46	0.48	0.14	0.97	3.11×10^9	8.70×10^7
Al (fcc)	200	6	2.02	21.9	0.25	8.52	0.48	0.14	0.96	4.66×10^8	8.70×10^7

2.4 Experiments at APS ID-7B

2.4.1 Experimental setup

In July of 2008 RMLFs of composition Al_3Zr were studied at the APS sector ID-7B. Pink-beam from an APS undulator A (pink-beam is the unfiltered output from the undulator and has a broad $\approx 2\%$ energy spread) was focused using rhodium-coated dynamically-figured Kirkpatrick-Baez (KB) mirrors [77]. The KB mirror box was approximately 23 cm long along the beam propagation direction. The foils were placed 22 cm from the downstream edge of the mirror-box. A millisecond stainless steel chopper reduced the heat-load on optical elements and was synchronized to the detector acquisition. At an energy of 8.1 keV with an upstream diamond (111) reflection monochromator of 6.5×10^{-5} bandpass an ion-chamber measurement gave a flux of 3.7×10^{11} photons/sec. Extrapolated to pink-beam with a bandpass of 2×10^{-2} estimates 1.1×10^{14} photons/sec. Eric Dufresne of the APS predicted a possible flux of 1.4×10^{15} photons/sec after transmission through beryllium windows and reflection from the KB mirror pair, using the XOP x-ray package[3]. The experiments were performed at an energy of 11 keV with a vertical spot-size at the sample of 54 μm FWHM. The data revealed that the flux estimates and anticipated spot-size were not accomplished, most likely due to a faulty KB mirror bender motor.

The detector face was positioned normal to the incident beam. The beam center and sample-to-detector distance were calibrated with silicon and Al_2O_3 powder standards.

In a process similar to that used at CHESS, images were acquired before reaction (referred to as $t = T_b$), during propagation of the reaction front, and after

[3] http://www.esrf.fr/computing/scientific/xop

cooling of the sample (referred to as $t = T_f \approx 5\,\mathrm{s}$). An adjustable delay was introduced between optical detection of the reaction front and PAD triggering to study the entire sample evolution. At greater delays longer exposure times were used, since the sample dynamics were assumed to be slower. The experiment was repeated with many foils to acquire sufficient statistics at all time points.

2.4.2 Results and interpretation

Figure 2.7 and Figure 2.8 show temporal progressions of detector images and radial integrations of the scattering intensity, respectively. At $t = T_b$ the image shows homogenous powder rings and results in a diffraction profile consistent with the presence of elemental aluminum and zirconium. The diffraction profile at $t = 55\,\mu\mathrm{s}$ shows the presence of the intermetallic Al_3Zr. These profiles indicate the phase progression proceeded as:

$$\mathrm{Al} + \mathrm{Zr} \rightarrow \mathrm{Al_3Zr}, \tag{2.10}$$

with Al_3Zr having formed promptly after passage of the reaction front. While the phase transformations may have occurred rapidly, evolution of the microstructure continued during cooling (as seen in Figure 2.7). The image at $t = 505\,\mu\mathrm{s}$ shows homogenous rings of intensity while the images at later times show spots.

When the x-ray beam illuminates many grains the Bragg spots cannot be individually separated and a homogenous ring is detected (image from $t = T_b$). If the x-ray beam illuminates only a small number of grains, individual spots are distinguishable (most apparent in image $t = T_f$). An increase in diffraction ring heterogeneity indicates fewer grains in the illumination volume and, hence typically larger grains.

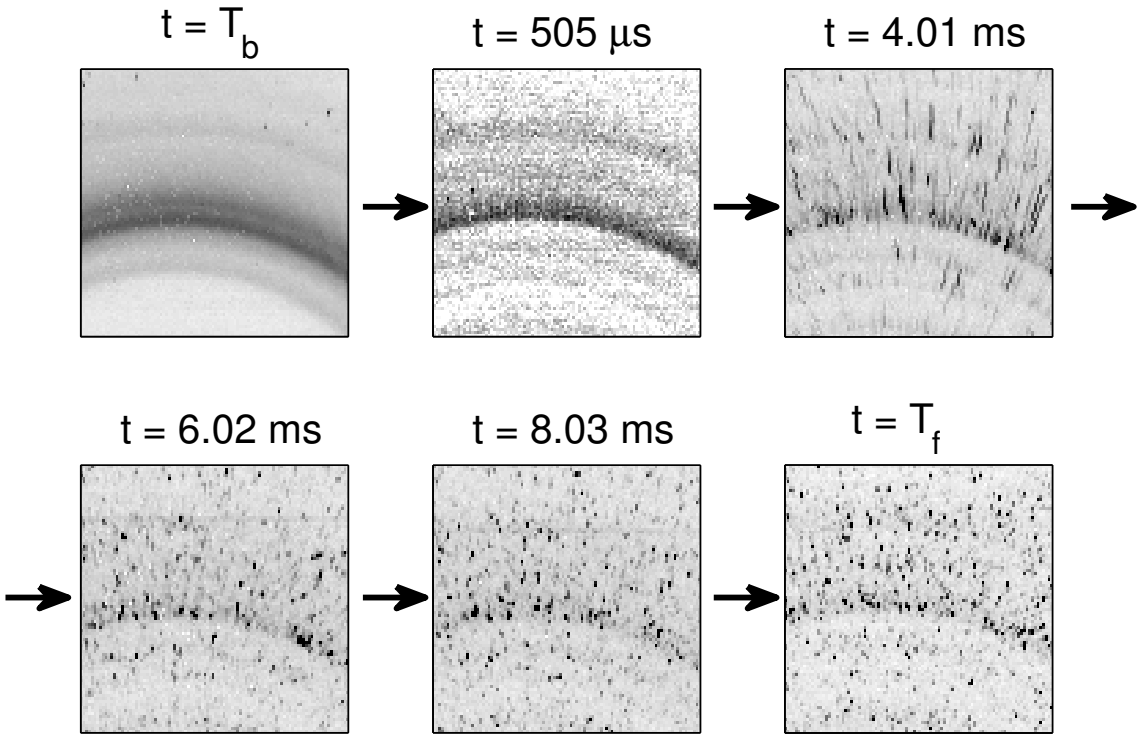


Figure 2.7: A progression of detector images with the time from trigger indicated at top. $t = T_b$ is an image from before the reaction while $t = T_f \approx 5$ s is an image after sample cooling. $t = 505\,\mu$s is a $250\,\mu$s exposure, all other images shown are 1 ms exposures.

Quantitative methods exist for estimation of crystallite size (Fourier inversion and the Scherrer equation) [68]. However, significant instrumental broadening prevented application of these techniques to this experiment.

The homogeneity of each ring was evaluated using a procedure illustrated in Figure 2.9 which presents data from $t = 505\,\mu$s and $t = T_f \approx 5$ s in the top and bottom rows, respectively. The image from $t = 505\,\mu$s shows smooth diffraction rings while the image from $t = T_f$ contains spots. This is quantitatively displayed by the distribution of pixel intensities shown in figures (b) and (e). The distribution in (e) has a higher number of low intensity pixels than (b) but the mean intensity is similar since (e) has a larger number of high intensity pixels (see inset). The last column, sub-figures (c) and (f), show the standard diffrac-

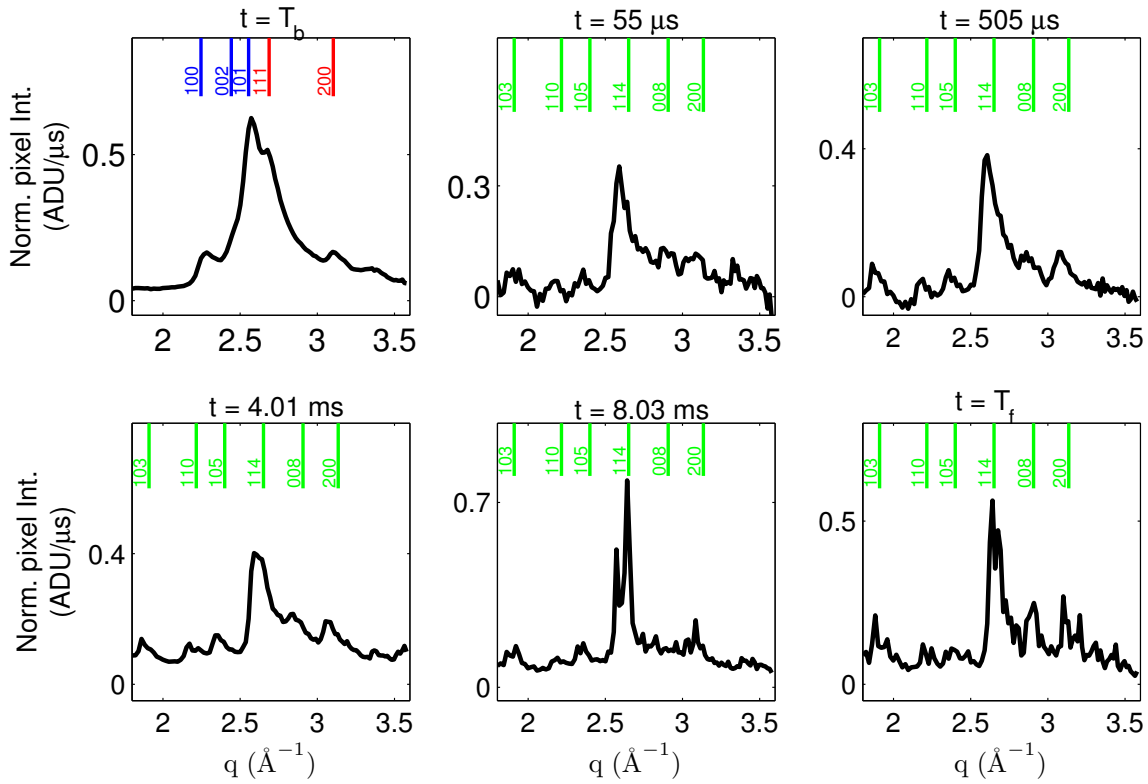


Figure 2.8: Diffraction profiles, with time from the trigger indicated at top, of before the reaction ($t = T_b$; 1 ms exposure), during the reaction, and after cooling ($t = T_f$; 1 ms exposure). t=55 μs is an average of five experimental runs with 50 μs exposure time. t=505 μs is an average of 17 experimental runs with 250 μs exposure time. The others are from single experimental runs. Notice that there is difficultly in phase identification after cooling when the patterns show less homogeneous rings and more isolated spots (as is the case for the panels from $t = 8.03$ ms and $t = T_f$). Index marks in red, blue, and green correspond to Al, Zr, and Al_3Zr, respectively, at room temperature.

tion profiles (mean pixel intensity measured at each momentum transfer, $I_\mu(q)$) and diffraction profiles from the 20th percentile of pixel intensities at each momentum transfer, $I_{20\%}(q)$.

The total volume of the Al_3Zr phase was tracked by the integrated area of the Al_3Zr(114) peak in $I_\mu(q)$ from $q = 2.54$ to $q = 2.69$ Å^{-1} ($A_\mu^{(114)}$). The density of grains was estimated by the integrated area of the Al_3Zr(114) peak in $I_{20\%}(q)$ ($A_{20\%}^{(114)}$) over the same q range. For the example in Figure 2.9 $A_\mu^{(114)}$ increased by a

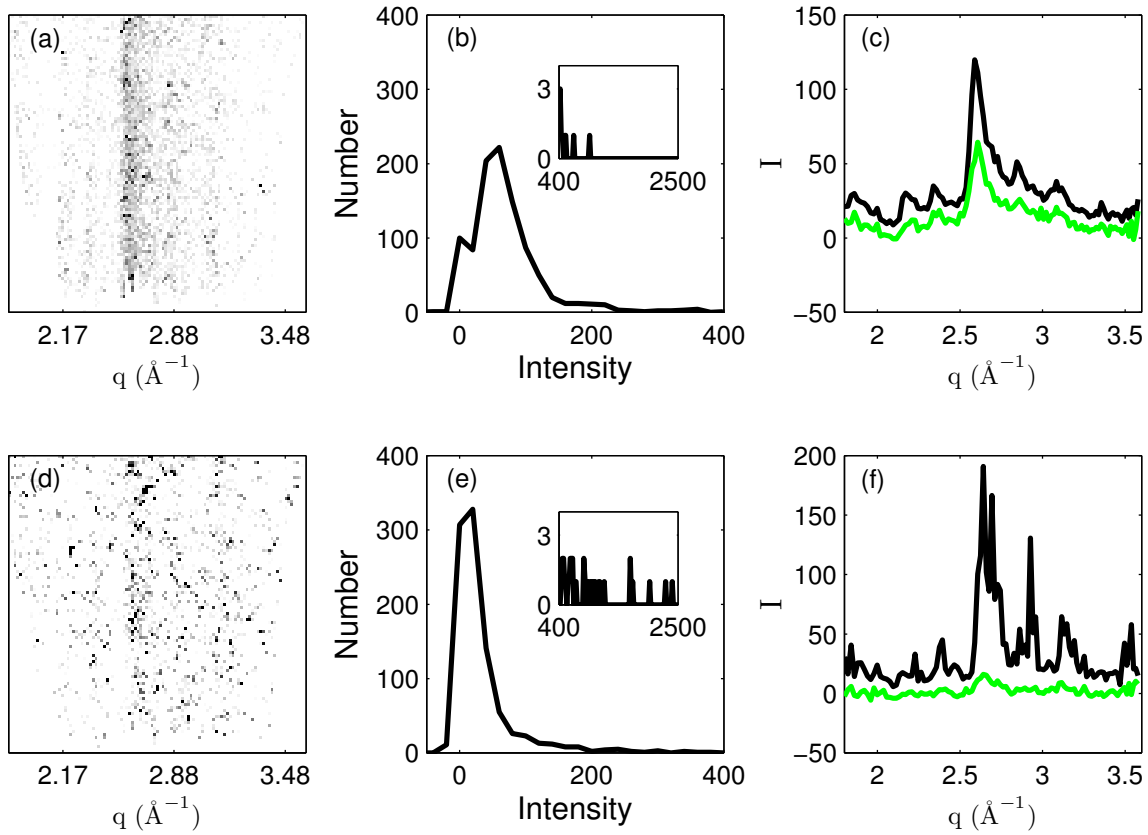


Figure 2.9: Demonstration of method to extract diffraction ring homogeneity from the distribution of intensity at each momentum transfer. The top row of sub-figures (a,b,c) is data from an image taken 505 μs after detection of the reaction front while the bottom row (d,e,f) is from the same sample after cooling. Sub-figures (a) and (d) show transformed images such that the horizontal direction represents the momentum transfer (q). After this transformation, diffraction rings become lines. The second column of sub-figures, (b) and (e), show histograms of the pixel intensities in the range of q = 2.54 to q = 2.69 Å^{-1}, which corresponds to the most intense diffracting plane, Al_3Zr(114). The insets have the same axes as the primary plots but focus on the distribution of pixels with intensities above the scale of the primary figure. Sub-figures (c) and (f) show the corresponding diffraction profiles with $I_\mu(q)$ in black and $I_{20\%}(q)$ in green.

factor of 1.1 from t = 505 μs to cooling. The integrated area from the twentieth percentile profile, $A_{20\%}^{(114)}$, decreased by a factor of 4.6 as grains grew. Following the procedures outlined by this example, the dynamics of grain growth are

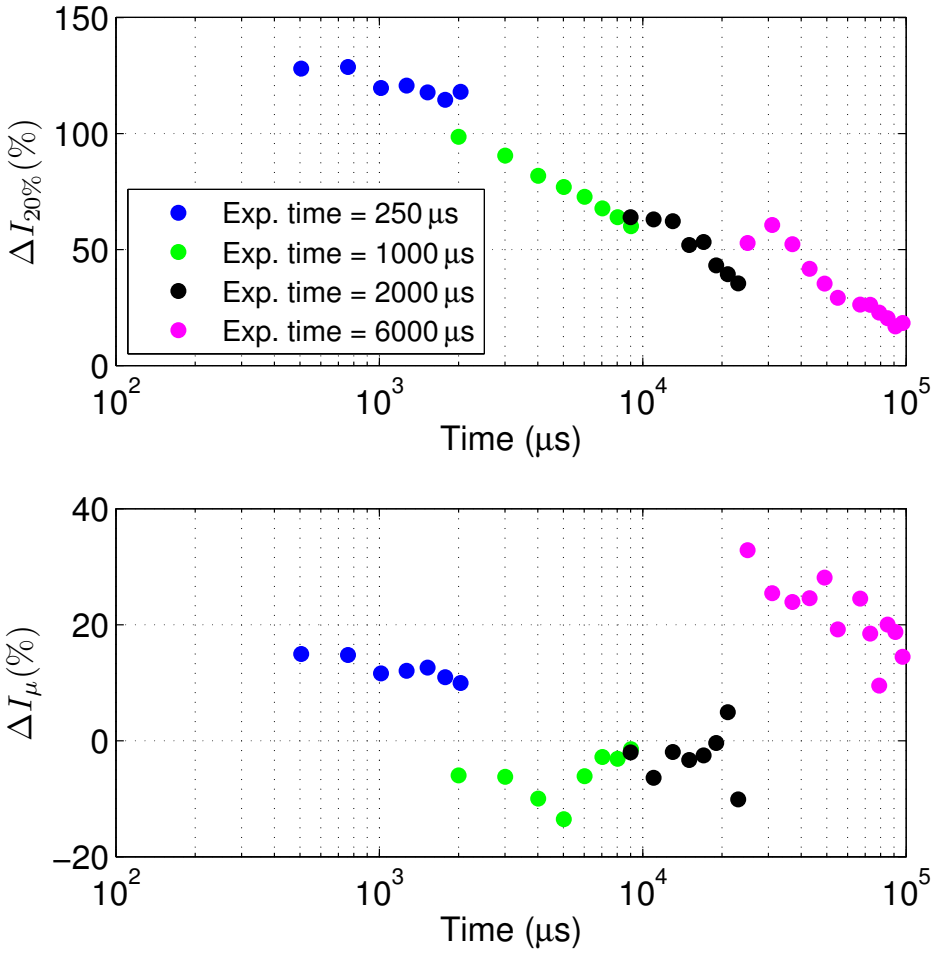


Figure 2.10: The top plot shows the percent difference, $\Delta I_{20\%}(t)$, of the peak area from the 20th percentile at the $Al_3Zr(114)$ crystallographic plane versus time. The bottom plot shows the percent difference from the diffraction profile derived from the radial mean.

studied through the entire time series.

The percent difference from the cooled foil versus time for the phase volume measure is defined as:

$$\Delta I_{\mu}(t) = 100 \frac{A_{\mu}^{(114)}(t) - A_{\mu}^{(114)}(T_f)}{A_{\mu}^{(114)}(t) + A_{\mu}^{(114)}(T_f)}. \tag{2.11}$$

Similarly, for the grain density measure:

$$\Delta I_{20\%}(t) = 100 \frac{A_{20\%}^{(114)}(t) - A_{20\%}^{(114}(T_f)}{A_{20\%}^{(114)}(t) + A_{20\%}^{(114)}(T_f)}. \tag{2.12}$$

These measures tracked versus time are shown in Figure 2.10. The downward trend with time in the top plot of Figure 2.10 shows the consumption of small grains. The rate of reduction in $I_{20\%}(t)$ decreases with time for two reasons. One, the temperature was decreasing, which left less thermal energy for diffusion, and two, fewer small grains were available to be consumed as grains grew. Trends in the total phase volume versus time were less clear. This suggests that, after initial formation, the volume of Al_3Zr crystallites remained constant as the sample cooled.

A complimentary evaluation of grain growth located and counted distinct spots in each image. This method involves scaling each image by the exposure time and then setting to zero any pixels below a constant threshold. After thresholding, regions of continuously connected non-zero pixels were considered a spot. In each image the number of spots and the intensity and area of each spot was found. The spot count extracted from images from cooled foils varied by less than $\sim 10\,\%$ across all exposure times (approximately 200 spots were found in each image). The normalized spot count was calculated as the spot count in the dynamic image divided by the spot count in the image taken after sample cooling ($t = T_f$). The normalized spot count is shown at the top of Figure 2.11 and the normalized spot average intensity is shown in bottom of Figure 2.11.

Discontinuities in normalized spot count are seen in Figure 2.11 and are expected when the exposure time is changed. Spots moved on the detector due to temperature change and grain rearrangement. Images with longer exposure times at equal time from detection of the reaction front showed fewer and larger spots because multiple spots intersect on the detector and are counted as one.

Some conclusions may be drawn from the data presented. The volume of the

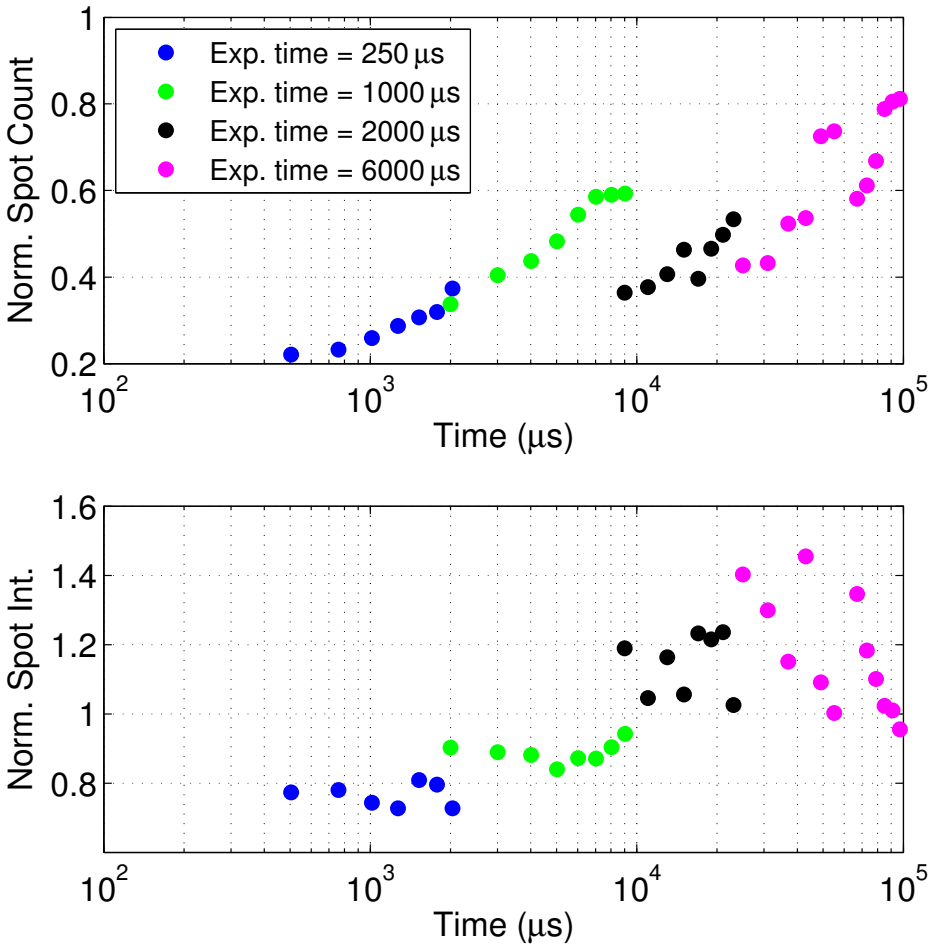


Figure 2.11: The top figure shows the number of spots found versus time normalized to the number of spots found at $t = T_f$. The bottom plot shows the same for the spot intensity. At lower spot densities (exposure times 250 μs and 1000 μs) the measures show fewer systematics due to a lower number of spots that overlaped.

Al_3Zr phase did not change considerably with time. Grain growth proceeded by consumption of small grains at a rate that decreased with time. The reduction in intensity of the homogenous diffraction ring began 2 ms after passage of the reaction front and continued throughout cooling for at least 100 ms. The number of spots detected increased by a factor of five from 500 μs to 100 ms. The normalized spot count increased with time but the average spot intensity did not show a clear trend versus time. The measures of spot counts and intensities

could be improved in future experiments by a modest reduction in the density of spots on the detector.

An interesting question to pursue is how the grain size distribution evolves during cooling. Are the grain boundaries of small grains more mobile? Do grains in certain orientations grow more slowly? The data do not seem to provide sufficient information to completely answer these questions. It does seem apparent that grains of the maximum size reached were found early in the cooling. As small grains were lost the number of detected grains increased but the average size of the detectable grains did not.

Grain growth is important to materials design as smaller grains are typical of stronger material [78]. The increased strength is because grain boundaries halt the motion of dislocations [79]. Rapid solidification is often used to induce small grain sizes [80]. Studies on grain growth with more quantitative results than those described above have been performed at the ESRF using a specialized x-ray diffraction microscope but at much slower rates (annealing times on the order of hundreds of minutes; minimum time resolution around 10 seconds) [81, 82, 83]. Our study using a PAD investigated crystal growth at cooling rates (10^3 K/s) more commensurate with rapid solidification.

The image from t = 4.01 ms shows radial streaks (see Figure 2.7). The streaks often span four pixels which implies a change in q of 0.05 Å^{-1} at q = 2.6 Å^{-1}. The change in q observed exceeded the lattice-parameter change expected from thermal expansion and occurred when the sample temperature was expected to be stable or cooling. Possibly, these streaks are due to compositional enrichment. Al_3Zr is stable with a composition range from 75%-100% Al [84]. Other studies have shown Zr to be the dominant diffusing species in this system [85] which implies that the Al_3Zr phase would start aluminum rich and subsequently be

enriched with zirconium. Aluminum is smaller than zirconium: the atomic volumes of Al and Zr are 16.60 Å^3 and 23.27 Å^3, respectively [86]. Streaks to lower q are consistent with enlargement due to Zr enrichment. Vegard's law is an empirical relationship that assigns a characteristic volume to each component of a binary mixture to determine the size of an alloy as a function of the composition [87]. This method calculates an anticipated fractional change in lattice parameter between Al_3Zr (100% Al) to Al_3Zr (75% Al) of:

$$\frac{r_{Zr} + 3r_{Al}}{4r_{Al}} = 1.03, \tag{2.13}$$

where r_{Zr} and r_{Al} are the radii of the zirconium and aluminum atoms. At $q = 2.6\,\text{Å}^{-1}$ a 3% change of lattice parameter would produce a change in q of $0.08\,\text{Å}^{-1}$ in reasonable agreement with the data. The linear size relation of Vegard's law is not obeyed by most metallic systems; a more precise estimation would use a King's table to determine the Al_3Zr lattice parameter versus Al composition [86], but the literature does not provide sufficient data to do so.

Another experiment at the APS with KB mirrors and pink-beam may lead to increased flux and a smaller spot-size if issues with the mirrors are resolved. Care must be taken to ensure that phase determination will be possible given the small number of Bragg reflections that will illuminate the detector. Continued development of techniques to study crystallite growth in a time-resolved manner would nicely complement time-resolved studies on phase nucleation.

The study of grain growth was not the expected result of the RMLF experiments attempted at the APS. Because of this, the experiment was not optimized to collect this data. For example, since the dynamics of grain growth were shown to be at millisecond time-scales a detector with in-pixel storage is not necessary. A PAD with 1 ms readout time could be used for continuous acquisition. The mixed-mode PAD described in chapter one would be appropriate.

With the mixed-mode PAD a continuous sequence of frames could be acquired for each foil from reaction initiation through cooling.

2.5 Detector modifications and developments

2.5.1 Noise and front-end gain

The RMLF experiments help guide detector design considerations. X-ray experiments are limited by two noise sources: Poisson fluctuations of the x-ray signal (shot-noise, dominant at high signal levels), and the read-noise of the detector pixels (dominant at low signal levels). The maximum accuracy obtainable, set by x-ray poisson statistics, is $\sqrt{N}/N$, given the detection of N x-rays. This limit has encouraged the design of detector pixels with a large saturation value. The maximum accuracy needed is inherently tied to the contrast of the experiment. Mass-density radiography experiments may have low contrast and subsequently require a large photon count per pixel. On the other hand, the RMLF experiments had large contrast between signal and background. For phase identification, the required result of the RMLF experiments, the quantity of interest was the existence and location of diffraction peaks and not precise peak intensity. Large photon counts per pixel were not acquired and the signal-to-noise was limited by the detector read-noise. For this experiment, a sacrifice of the pixel saturation level would improve the minimum possible exposure time since the sensitivity at low illumination would be increased. Higher sensitivity is accomplished by a reduction in the feedback capacitance of the front-end amplifier in the PAD pixel. Since the tradeoff between read-noise and saturation level depends on the experiment, the opportunity to optimize the detector sensitivity electronically is valuable. The work in this dissertation does that by the

implementation of an electronically adjustable gain at the pixel front-end.

2.5.2 Signal induced offset

The RMLF experiments encountered a problematic aspect of the 100×92 prototypes. X-ray signal incident on the detector before image acquisition has been observed to shift the detector's pedestal level [48]. During the RMLF experiments at CHESS the signal induced background shift was accounted for by acquisition of 1 μs exposures, short enough that the background shift was the dominant signal. Once measured the aberrant signal was removed from the diffraction patterns [88].

When initially encountered in high-flux tests, this shift was attributed to a pixel input current ($\sim 0.3\,\mu$A) that induced a shift because it was a significant fraction of the static bias current of the input amplifier [48]. In the RMLF experiments this anomalous response could not have been from an overwhelmed input stage since the maximum signal current was on the order of 100 pA. Possibly, at least for the RMLF experiments, the cause was conversion of x-rays that passed through the detector layer and converted in the CMOS substrate. If the charge produced was collected by sensitive nodes in the pixel electronics (for example, by transistor switches connected to storage capacitors) a shift would have resulted. Depending on the experiment, the 'exposure time' of the anomalous signal may far exceed the actual exposure time. This was the case for the RMLF experiments at CHESS, as the time of arrival of the reaction front was uncertain and required the x-ray shutter to be opened while the detector waited for a trigger. At the APS the reaction initiation was prompt and synchronized to the shutter so that the time that x-rays were incident on the detector before exposures was reduced. The APS data did not require adjustment for the signal

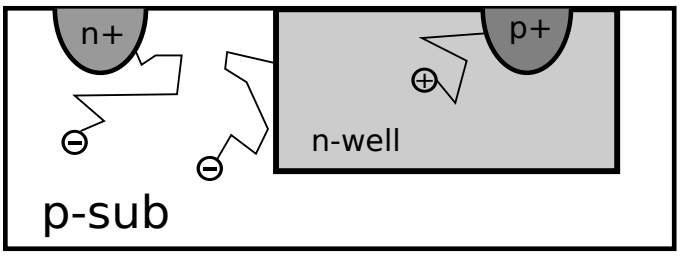


Figure 2.12: Mechanisms of charge collection in the readout ASIC. Electrons produced by x-ray conversion in the p-substrate can be collected by either n+ transistor diffusions or by n-wells. Holes from x-ray conversion in the n-well can be collected by p+ transistor diffusions.

induced background shift.

Figure 2.12 shows mechanisms of charge collection in the readout ASIC. Collection of electrons by n+ transistor diffusions and collection of holes by p+ transistor diffusions may couple to sensitive parts of the pixel electronics. Collection of electrons by an n-well will be drained to the supply the n-well is tied to. One method to reduce collection by n+ diffusions of NMOS transistors is the fabrication of the NMOS transistors in a separate p-well. 'Twin-tub' processes allow for this: NMOS transistors are fabricated in a p-well built on a lightly doped epitaxial p-layer. A potential barrier of height, $V_{barrier}$, is present at the p-well substrate interface [89]:

$$V_{barrier} = \frac{kT}{q} \ln \frac{N_{ptub}}{N_{epi}}, \tag{2.14}$$

where N_{ptub} is the doping of the p-well and N_{epi} is the doping of the epitaxial layer. The barrier restricts electrons in the epitaxial layer from entering the p-well. The reduction of parasitic collection by NMOS transistors with twin-tub technology is an advantage of epitaxial CMOS processes over the non-epitaxial processes the Cornell x-ray detector group has typically favored. Another approach would include additional n-wells to collect electrons and prevent them from reaching transistor n+ diffusions.

The easiest solution is to configure control signals so all storage capaci-

tors are reset before exposure acquisition. However, during readout, storage capacitors must be disconnected and collected substrate charge could lead to unwanted signal. Since collection in the CMOS electronics is difficult to model and predict experimental measurements will be made of the cross-section for x-ray conversion later in this dissertation.

2.5.3 High-speed analog integrating 1D detector

With random crystallite orientation and a large x-ray beam that samples many grains, the diffraction intensity is symmetric about the azimuth. Hence, if only phase identification is desired, a one-dimensional detector array could suffice. Imagine a design with silicon detector strips (around 5 mm wide with 100 μm pitch) individually wire-bonded to a bonding pad on a readout ASIC. The readout ASIC would contain analog integrating pixels similar to those in the 100x92 detector but modified to allow simultaneous integration and readout [90]. An analog-to-digital converter (ADC) would be placed at each pixel to remove the readout bottle-neck and allow for continuous data acquisition. ADCs have been implemented at each column of video-rate CMOS imaging arrays (a single camera chip has been designed with over 8,000 ADCs). One example used a 14-bit successive approximation ADC 8.4 μm wide, with a 1.7 μs conversion time, and 41 μW power consumption [91]. A strip of 600 pixels using a similar ADC on the ASIC would require only 25 mW. Given the less demanding pitch requirement for this proposed detector the ADC could be designed to be larger, faster, and consume more power than the example. At 2 bytes stored per conversion, data would be produced at a rate of 600 MB/s. This data could be buffered into a Double Data Rate 3 (DDR3) SDRAM (synchronous dynamic random access) build-on module to an FPGA board [92]. Memory modules currently available

feature sufficient data rates and a capacity of 4 GB which would allow continuous acquisition for 6.6 s before write to more permanent hard-drive storage would be required. This proposed detector could continuously stream a few million powder diffraction curves at microsecond resolution. The large solid-angle per pixel may improve the noise performance at short integration times.

2.6 Conclusion

This chapter described the study of propagating reaction fronts within multilayer foils using x-ray diffraction. The fronts moved past a fixed point in tens of microseconds, which required a fast x-ray detector and a focused, intense x-ray beam. The phase progression of three different foil compositions were studied at CHESS A2 station. The high-heating rates and limited time for nucleation of unabated reaction fronts proved important as the results differed from experiments at slower heating rates. At the APS the studies were extended to time-resolved crystallite growth. The results followed grain growth through cooling and introduced a new experimental approach for the study of recrystallization at high cooling rates. Lessons were drawn from the experiment for future time-resolved pixel array detector design.

CHAPTER 3

SINGLE-BUNCH PAD BASICS AND FIRST TEST-CHIP DESIGN AND MEASUREMENTS

3.1 Introduction

This chapter presents the fundamentals of high-speed analog PAD design and shows test results from a CMOS chip. Front-end amplifier design is considered in relation to the efficiency of collection of the charge from the detector layer and the speed of measurement. The pixel feedback and load capacitance can be manipulated in the design process so expressions are presented to quantify the effect of capacitor sizes on performance metrics. Single bunch experiments may have limited signal per bunch and thus benefit from pixel circuitry that allows for addition of distinct temporal windows before readout (termed accumulation). Two circuits to accomplish in pixel accumulation are described, incorporated in the test chip, and evaluated. Capacitors as memories are central to analog PAD design. Charge injection and switch leakage, which degrade analog memories, are described and mitigation techniques are presented. A testbench is a simulation environment that allows for straightforward evaluation of amplifier designs. To ease comparisons of amplifiers, software for a testbench that extracts performance parameters relevant to PAD design was created and is tabulated in this chapter. Experimental measurements of the test-chip confirmed functionality and probed for flaws.[1]

[1]Parts of this chapter have been published. *IEEE Transactions on Nuclear Science*, "An Accumulating Pixel Array Detector for Single-Bunch Synchrotron Experiments", Lucas J. Koerner, Mark W. Tate, Sol M. Gruner [93].

3.2 Single-bunch PAD basics

3.2.1 Front-end amplifier

A basic schematic of a PAD front-end amplifier is shown in Figure 3.1. PAD pixel circuits must account for explicit capacitive coupling between pixels through the monolithic detection layer. Capacitive cross-talk between pixels is prevented if the voltage at the electrode (node IN) is held stable as signal current is integrated. To do so a feedback amplifier is used. In the sections that follow, a generic front-end amplifier configured as in Figure 3.1 is considered and the charge collection efficiency, response speed, and factor of amplifier noise sampled at the output are quantified versus the transconductance and output resistance of the amplifier and the sizes of C_{IN}, C_F, and C_L.

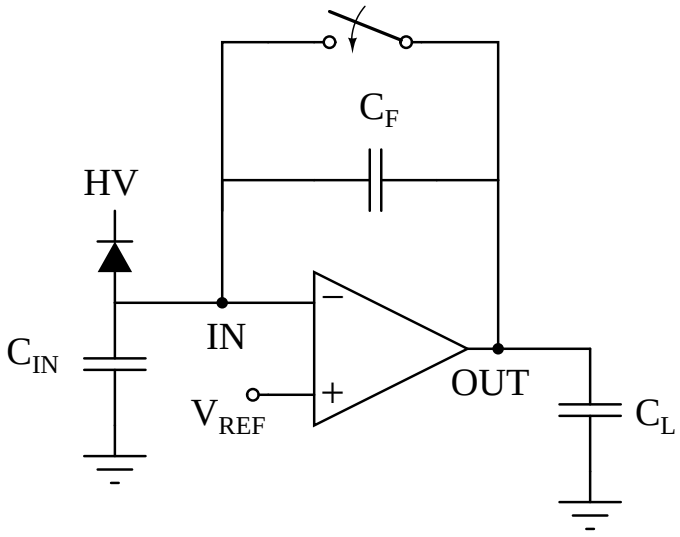


Figure 3.1: Schematic of a PAD front-end. Photocurrent enters from the reversed biased diode and is integrated across the feedback capacitor, C_F. The amplifier feedback maintains the electrode bias (node IN) at V_{REF}.

3.2.1.1 Charge collection efficiency

The fraction of charge that is integrated across the feedback capacitor, C_F depends on the amplifier gain and the pixel capacitor values. The negative feedback from the amplifier enhances the charge collection of capacitor C_F. For an amplifier open-loop gain of A, the feedback capacitance is enchanced to a value of $(1 + A)C_F$. The change of the voltage at node 'IN' is

$$\Delta V = \frac{Q_{IN}}{C_{IN} + (1 + A)C_F}, \tag{3.1}$$

where Q_{IN} is the input signal charge, and C_{IN} is the lumped capacitance of the amplifier input, the detector layer, and the connecting bump-bond. The fraction of charge collected by the feedback capacitor (CCE) is

$$CCE = \frac{(1 + A)C_F}{C_{IN} + (1 + A)C_F}. \tag{3.2}$$

3.2.1.2 Settling time and slew rate

The bandwidth of the amplifier determines the speed at which small-signal voltage deviations at the storage capacitance, C_L, are settled. The slew-rate of the amplifier sets the time required for a large-signal voltage change at the load capacitance. The small-signal response of the amplifier may be represented as in Figure 3.2. The output resistance of the amplifier is given by $R_o = dV_{OUT}/dI_{OUT}$ and the amplifier transconducatance is given as $G_m = dI_{OUT}/dV_{IN}$. The DC voltage gain is

$$A = R_o G_m = \left(\frac{dV_{OUT}}{dI_{OUT}}\right)\left(\frac{dI_{OUT}}{dV_{IN}}\right). \tag{3.3}$$

The settling-time of the small-signal model shown in Figure 3.2 is [94]

$$\tau = \frac{C_O}{\beta_F G_m}. \tag{3.4}$$

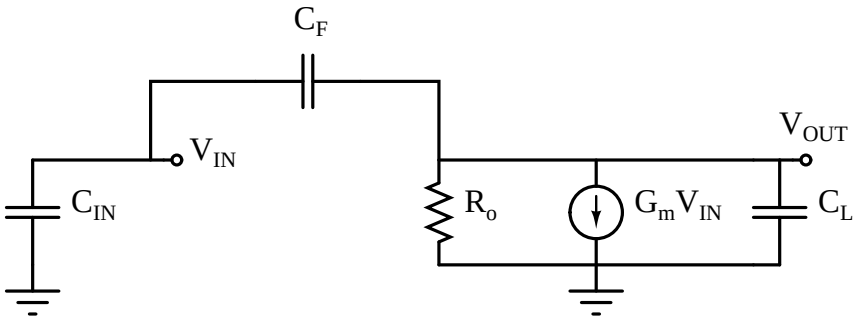


Figure 3.2: Small-signal model of the front-end CTIA.

C_O is the parallel combination of the load capacitance and the series combination of the feedback and input capacitances:

$$C_O = C_L + \frac{C_{IN}C_F}{C_{IN} + C_F}, \tag{3.5}$$

and β_F quantifies the feedback:

$$\beta_F = \frac{C_F}{C_F + C_{IN}}. \tag{3.6}$$

These calculations are made with the reasonable assumption that, $A \gg \beta_F$ [94]. The time-constant may be modified to read:

$$\tau = \frac{C_L C_F + C_L C_{IN} + C_{IN} C_F}{G_m C_F}. \tag{3.7}$$

Equation 3.7 shows the time-constant to decrease with an increase in the feedback capacitance with a sensitivity given as

$$\frac{d\tau}{dC_F} = \frac{-C_L C_{IN}}{G_m C_F^2}. \tag{3.8}$$

Also, the time constant is inversely proportional to the amplifier transconductance which motivates maximization of the transconductance.

Next, some practical values for the amplifier parameters are considered to estimate the small-signal settling times. A feedback capacitor of 500 fF gives a full-well at an energy of 8 keV of 2140 x-rays with a front-end amplifier swing

of 1.5 V (with a signal per x-ray of $\Delta V_{\text{x-ray}} = 700\,\mu$V). A full-well of 2140 x-rays allows for a Poisson limited accuracy of $\sqrt{2140}/2140 = 2.2\%$ per-pixel in a single frame. The input capacitance, C_{IN}, is anticipated to include 60 fF due to the detector layer [95], 55 fF due to the amplifier input devices and 15 fF due to the input bump-bonding pad, which totals 130 fF. A small load capacitance (C_L) is favored for speed and area considerations while a larger load capacitance reduces sampled noise and limits corruption of stored voltages from leakage. For this example, a capacitor value of $C_L = 300$ fF is selected.

The transconductance of a transistor depends upon the drain current through it. An important metric that emphasizes the tradeoff between speed and power dissipated is the transconductance to current ratio. This ratio is maximized for a transistor biased in deep weak inversion at $g_m/I_D = 1/(n\phi_T) = 28.5\,\text{V}^{-1}$, where ϕ_T is the thermal voltage and $n \approx 1.3$ is the reciprocal slope factor [96]. Simulations show $G_m/I_{tot} \approx 5\,\text{V}^{-1}$ for a differential folded cascode amplifier (each transistor at the input has a drain current of $I_{tot}/4$, where I_{tot} is the total current dissipated by the amplifier). Single-ended input amplifiers and single-branch amplifiers (for example a telescopic cascode) would have a larger G_m/I_{tot} value but are not explored due to poor power supply noise rejection and radiation robustness of single-ended input amplifiers and limited voltage swing of single-branch amplifiers. Settling to M-bit accuracy requires $t_{settle} = \tau M \ln(2)$. Small-signal settling to 8-bit accuracy (8-bit accuracy, 0.4%, comfortably exceeds the Poisson limited accuracy of the full-well acquisition of 2000 x-rays, 2.2%) given the capacitor values and the transconductance to current ratio discussed above requires a time of,

$$t_{settle} = \frac{565}{I_{tot}}[\text{ns} \cdot \mu\text{A}]. \tag{3.9}$$

The time to settle the output voltage after an impulse of x-ray induced charge is the sum of the small-signal settling time shown in equation 3.9 and the time required to slew the change in output voltage (large-signal response). Here slewing of large input signals is considered. For this discussion the detector layer is considered to provide a delta-function current impulse; in reality a current is seen at the pixel electrode with a duration defined by the hole collection time. Given standard operating parameters of a 500 μm thick silicon detection layer the hole collection time is constrained at less than 30 ns [34]; thus, as discussed in chapter one, charge collection will not limit time resolution in a way that prevents single-bunch imaging. Immediately after arrival of a charge impulse, Q_{IN}, the pixel is considered to contain only the three capacitors (C_F, C_L, C_{IN}), as the amplifier has a finite response time (see Figure 3.3). The voltage at the front-end output increases by [95]:

$$\Delta V_{OUT} = Q_{IN} \frac{C_F}{C_F C_L + C_F C_{IN} + C_L C_{IN}}. \tag{3.10}$$

The pixel input increases similarly as

$$\Delta V_{IN} = Q_{IN} \frac{C_F + C_{IN}}{C_F C_L + C_F C_{IN} + C_L C_{IN}} \tag{3.11}$$

and needs to be maintained below the level that forward biases the source-bulk junction of the PMOS Φ_F switch, otherwise signal charge is lost to the supply.

The output voltage eventually settles to $V_{REF} - Q_{IN}/C_F$ which gives a voltage to slew of

$$V_{SLEW} = \Delta V_{OUT} + \frac{Q_{IN}}{C_F}. \tag{3.12}$$

The capacitance to slew is the addition of the load capacitance and the series combination of the feedback and input capacitances for a slew-rate, SR, of

$$SR = \frac{I_{load}}{C_L + (C_F C_{IN})/(C_F + C_{IN})} \tag{3.13}$$

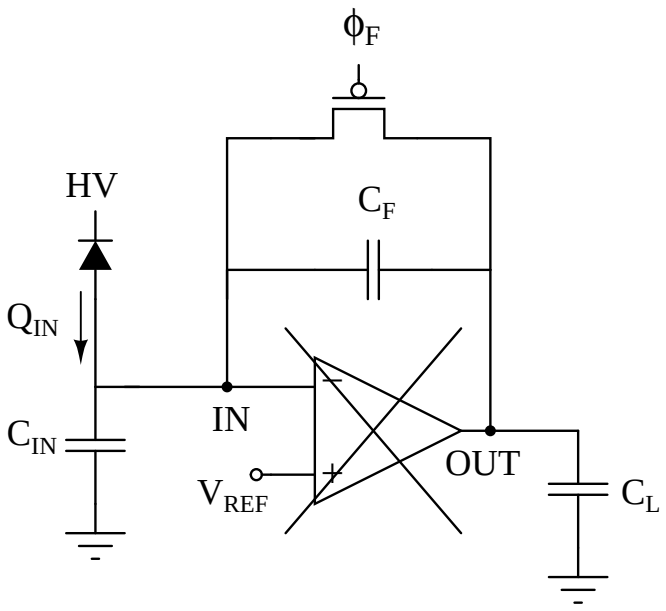


Figure 3.3: A schematic to show the capacitive divider at the front-end to determine the voltage jumps at the input and output after an input charge pulse. For the initial transient the amplifier is ignored.

where I_{load} is the current the amplifier supplies to the load during a slewing event. The time for slew is then V_{SLEW}/SR:

$$t_{slew} = \frac{Q_{IN}}{I_{load}} \frac{C_F + C_L}{C_F}, \tag{3.14}$$

with a sensitivity to the feedback capacitance of

$$\frac{dt_{slew}}{dC_F} = \frac{-Q_{IN}C_L}{I_{load}C_F^2}. \tag{3.15}$$

For a given input charge a large feedback capacitance reduces the time for slew. The time for slew in equation 3.14 is a simplification because the voltage difference at the input terminals varies throughout settling. At times the voltage difference is not large enough for the amplifier to supply maximum current to the load.

Summing the time for small-signal settling, (3.9), and the time for slewing, (3.14), gives the total 8-bit settling time,

$$t_{total} = \frac{565}{I_{tot}}[\text{ns} \cdot \mu\text{A}] + \frac{3.2 \cdot Q_{IN}}{I_{tot}} \left[\frac{\text{ns} \cdot \mu\text{A}}{\text{fC}}\right], \tag{3.16}$$

where an amplifier that supplies half of the quiescent current to the load during a slewing event has been assumed ($I_{tot} = 2I_{load}$). Given an input signal of 2140 x-rays of 8 keV energy (750 fC) the combined slew and settle time is:

$$t_{total} = \overbrace{\frac{565}{I_{tot}}[\text{ns} \cdot \mu\text{A}]}^{\text{small-signal}} + \overbrace{\frac{2400}{I_{tot}}[\text{ns} \cdot \mu\text{A}]}^{\text{slew}}. \tag{3.17}$$

For large input signals the time for slew dominates the total settling time.

3.2.1.3 Amplifier noise transfer

The transfer of the amplifier thermal noise to the output depends upon the capacitive parameters and the amplifier transconductance. Following reference [94] the transfer function from node V_{REF} in Figure 3.1 to the output is given as

$$H(s) = \left(\frac{A}{1 + \beta_F A}\right)\left(\frac{1}{1 + s\tau}\right), \tag{3.18}$$

where s is the complex frequency variable from the Laplace transform. The amplifier transistor noises are represented as a noise voltage source at the non-inverting input with white power spectral density (PSD) of S. The mean square output noise is calculated as the integral across all frequencies of the noise PSD shaped by the transfer function of equation 3.18

$$v_{OUT}^2 = \int_0^\infty S(f)|H(j2\pi f)|^2 df = S\left(\frac{1}{4\beta_F^2 \tau}\right) = S\,\frac{G_m(C_F + C_{IN})^2}{(C_F + C_{IN})C_F C_L + C_F^2 C_{IN}}, \tag{3.19}$$

where $A \gg \beta_F$ has been assumed.

Before an exposure the switch in Figure 3.1 is closed to clear charge across C_F. A noise charge is left at node IN when the reset switch is opened to begin an exposure. The derivation of the reset noise at this node is extensive; see [97] for detailed considerations and a discussion of reset-noise reduction techniques. A reasonable approximation is that the RMS noise charge (Q_n) is given by [97]:

$$Q_n \approx \sqrt{kTC_{IN}} + \sqrt{kTC_F}. \tag{3.20}$$

The output voltage signal per x-ray is proportional to the inverse of the feedback capacitance ($\Delta V_{x-ray} \propto 1/C_F$) . A smaller feedback capacitance reduces the CTIA feedback factor and increases the noise voltage at the output. Due to the noise dependence on the feedback capacitance, the low-illumination signal-to-noise ratio has a more subtle dependence upon the feedback capacitance than $\propto 1/C_F$, given an imager with noise dominated by the thermal noise of the input amplifier. Consider a comparison of $C_F = 50\,\text{fF}$ and $300\,\text{fF}$. Equation 3.19 yields an output noise transfer 2.9 times higher for the smaller 50 fF integration capacitance. The low-end signal-to-noise ratio, then, is only a factor of 2.05 better for $C_F = 50\,\text{fF}$ versus $C_F = 300\,\text{fF}$. In contrast, a factor of 6 is expected if the dependence of the output noise on the feedback capacitor is neglected.

3.2.2 Accumulation

The pixels are designed so that capacitors can be re-addressed and signal added without reading out the device. This addition may happen after either signal acquisition into a different capacitor or electronic shuttering of the x-ray signal. A frame (output from a single readout) may thus be built from temporally separated acquisition windows. Each distinct window is referred to as an accumulation. Mathematically, the result of this circuit may be represented as:

$$\mathrm{F_n} \propto \overbrace{\int_{t_1}^{t_2} I_{IN}(t)dt}^{\text{Accum.}} + \overbrace{\int_{t_3}^{t_4} I_{IN}(t)dt}^{\text{Accum.}} + \overbrace{\int_{t_5}^{t_6} I_{IN}(t)dt}^{\text{Accum.}} + ..., \tag{3.21}$$

where $I_{IN}(t)$ is the current induced by x-ray conversion at time t, $t_{i+1} > t_i$, F_n is one of N output frames from the pixel, and 'Accum.' indicates that the integration of the input signal from t_n to t_{n+1} is a distinct accumulation. In the example of equation 3.21 the x-ray signal may be stored on a different frame element or

discarded during the time between t_2 and t_3 and the time between t_4 and t_5.

The signal in a single-bunch experiment may not be sufficient to surpass the read-noise of the detector. Accumulation may overcome low signal levels as it accomplishes in-pixel noise averaging before readout given a repeatable signal. For example, multiple shots from single-bunches were needed for the Laue protein crystallography experiments with myoglobin at the ESRF [5]. This required a high-speed mechanical chopper. With this PAD described here electronic shuttering is possible so that mechanical chopping of the x-ray beam is not required.

The accumulation functionality may be applied to the study of a sample driven by an oscillatory stimulus. Each storage frame would accumulate x-ray signal during different phases of the stimulus. A second possible application is the study of systems that produce distinct asynchronous triggers. The detector control system would be designed to link each frame to a unique trigger type. Following the detection and classification of a trigger, the detector would accumulate x-ray signal onto the appropriate frame element.

In-pixel accumulation has been implemented in two-dimensional array time-of-flight (TOF) imagers to improve the signal-to-noise ratio before readout. Reference [98] synchronized a pulsed illumination source to integration windows. The signal collected versus the time-delay between the integration window and the pulsed illumination measured the light propagation time. The signal from one pulse was not sufficient so accumulation was used to improve the signal-to-noise. The pixel used a fully-differential switched capacitor amplifier that performed discrete time summation and correlated double sampling filtering [99].

Similar circuit architectures have been used as a demodulator of the input optical signal intensity. A TOF range camera used a modulated light source and

an accumulating pixel architecture to extract the phase of intensity modulation of the returned optical signal which encoded the object distance [100]. This camera was fabricated in a CMOS/CCD process and used CCD charge transfer mechanisms to accomplish the in-pixel accumulation. The pixel had only one-storage site so that pixel values were read in between the collection of each phase of the modulated signal. Other work by Seitz developed a lock-in CCD with four storage sites per pixel [101].

As noted in [100] accumulation allows for sensitivity to discrete frequencies of intensity modulation in a fashion similar to a lock-in amplifier. The minimum integration time of an accumulation is set by the pixel speed which allows for measurement of frequencies beyond the limit set by the readout time. In chapter five frequency selectivity is developed further and used to extract a measure of the power spectral density of the input intensity.

3.2.3 Circuits for accumulation

Two paradigms explored for an accumulating charge integrating readout ASIC are shown in Figures 3.4 and 4.5. Both of these pixel architectures have been fabricated and tested. The first approach uses a switched-capacitor storage stage (shown in Figure 3.4) at the pixel back-end. After closing all switches to clear charge across capacitors the pixel timing for accumulating onto storage element C_{S1} proceeds as follows:

- All Φ_S opened, Φ_F, Φ_R closed.
- Φ_F opens.
- Φ_R opens sampling the reset of the front-end and beginning integration. Soon thereafter Φ_{S1} closes.

- Exposure time: integrate charge Q_{IN}.
- Φ_{S1} opens ending the integration and leaving a voltage:
  $V_{REF2} + (Q_{IN}/C_F)\,(C_1/C_{S1})$ at $\mathrm{PIX_{OUT}}$.

The above approach accomplishes in-pixel correlated double sampling since the front-end reset voltage is sampled by the storage stage (in the third step). The noise reduction from correlated double sampling is limited in the actual realization of the circuit within a PAD pixel. This is because both the sizes of the front-end feedback capacitor and the sampling-stage capacitors and the speeds of the amplifiers are similar. Hence, the noise imparted by the sampling-stage when the front-end reset value is measured is expected to be similar to the noise imparted during front-end reset.

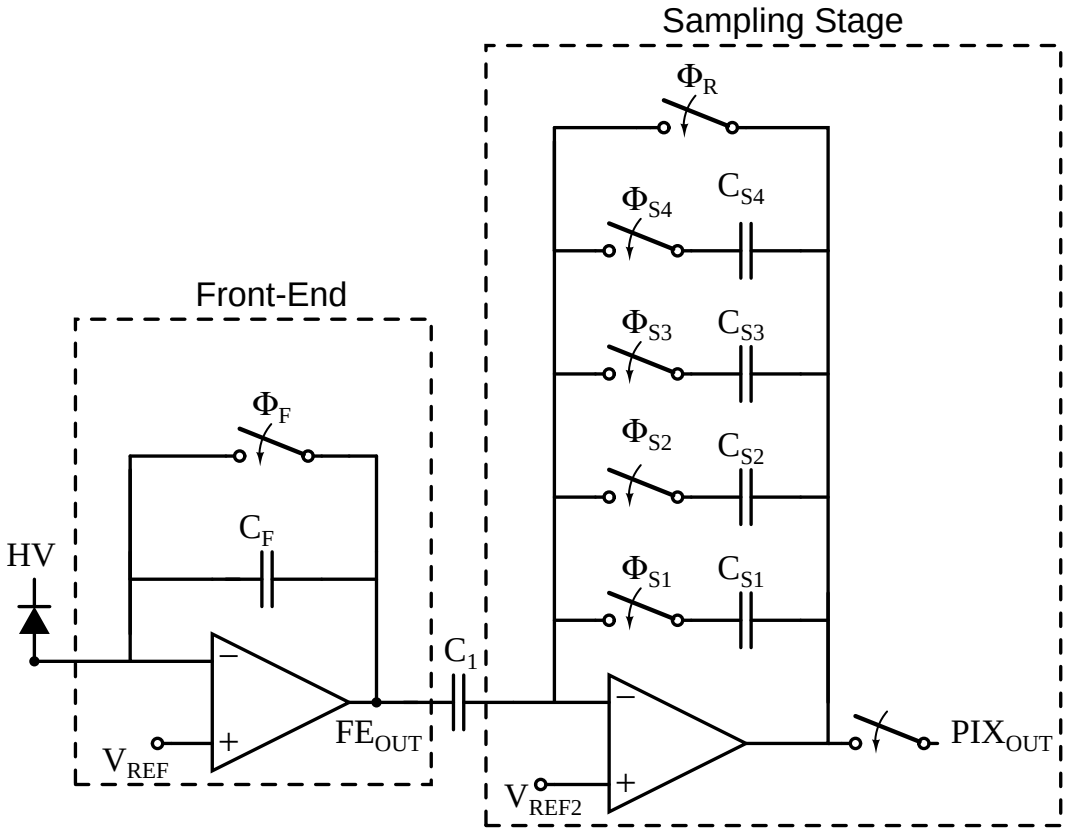


Figure 3.4: A schematic of the pixel that uses a switched-capacitor discrete-time integrator to accomplish accumulation in the pixel.

This configuration has a gain at the sampling-stage of C_1/C_{S1}. If the front-end amplifier noise is dominant the swing of the sampling-stage may be extended by selecting a gain less than one without a reduction of the signal-to-noise ratio. Unfortunately, for less than unity gain the storage capacitor must be the largest capacitor. This capacitor is replicated in a quantity equal to the number of frames desired, which makes a sampling configuration with a gain of less than one costly in terms of pixel area.

The architecture with a switched capacitor integrator storage stage uses a signal chain that converts the input charge to a voltage signal at FE_{OUT}. To add the voltage produced at the front-end output the signal is then converted back to the charge domain. The intermediate conversion step adds extra complexity and could be eliminated if addition were to occur at the front-end amplifier. This is the motivation of the second approach which uses the front-end integration capacitor as the storage element during accumulation (shown in Figure 4.5). Accumulation is accomplished via switches Φ_{F1-4}. At the end of each frame the front-end output is captured by one of an array of capacitive storage elements (C_{S1-4}) for later readout. During readout switch Φ_{SE} is opened to disconnect the front-end from the sampling stage. Then Φ_{RE} is closed, Φ_{BP} opened, and switches Φ_{S1-4} are used to connect the correct storage capacitor across the readout amplifier to buffer the stored voltage onto the readout bus. A final version of the detector would include more storage capacitors to increase the number of distinct temporal snap-shots when accumulation is not utilized.

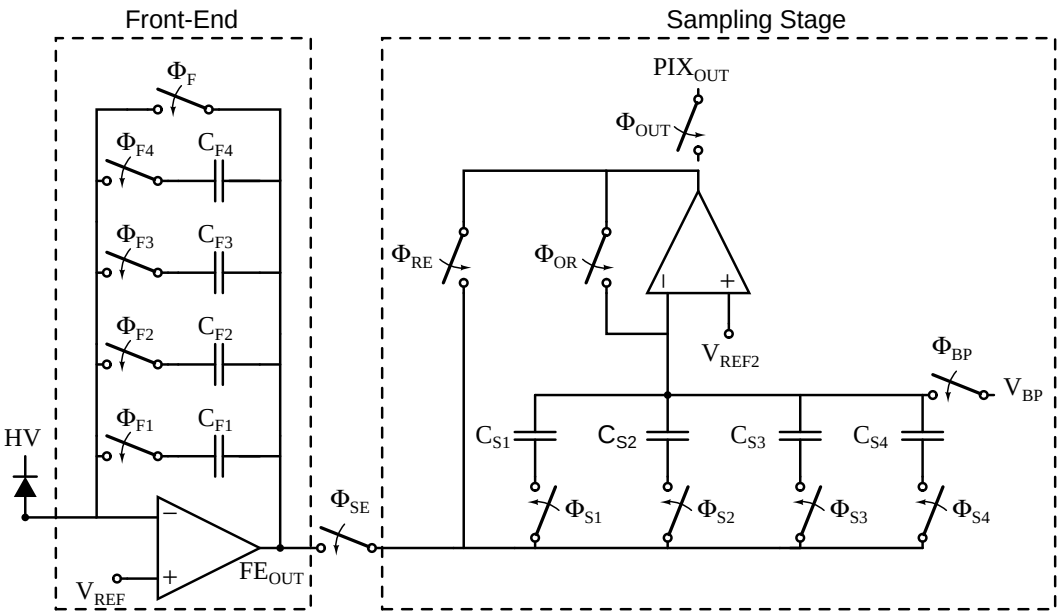


Figure 3.5: A schematic of the pixel that incorporates accumulation at the front-end integration capacitors. The storage stage captures successive frames with or without the use of accumulation at the front-end. Two-bit front-end charge-to-voltage gain selection is possible when accumulation is not used.

3.2.3.1 Charge injection

The accumulation techniques require transistor switches coupled with capacitors to sample voltages. A non-ideal effect introduced when switches transition is the injection of charge carriers from the transistor channel and from capacitive coupling of the gate control signal through the gate to source/drain overlap capacitance (C_{OV} in Figure 3.6). This charge injection is problematic for two reasons. First, the pixel saturation value may be approached after fewer integrated x-rays if significant charge is injected from the switches during each accumulation. Second, if the quantity of charge injected from the switches depends upon the pixel voltages non-linearity is introduced to the pixel response.

Switch charge injection is mitigated by the use of smaller switches that inject less charge up to the limit set by the maximum switch resistance for

speed considerations. The resistance of a MOS transistor in the linear region ($V_{DS} \ll 2(V_{GS} - V_{TH})$) is given as

$$R_{on} = \frac{1}{\beta_{N,P}(V_{GS} - V_{TH})}, \tag{3.22}$$

where V_{TH} is the transistor threshold voltage and $\beta_{N,P}$= $\mu_{N,P}C_{ox}(W/L)$, with $\mu_{N,P}$ the mobility of carriers in an NMOS or PMOS device, C_{ox} the gate-oxide capacitance, and W/L the ratio of the transistor width to length[2]. In the CMOS process used for this chip design a PMOS switch with an aspect-ratio of 8 passes an input voltage of 2.0 V with an on-resistance of ~2 kΩ. A rule of thumb to ensure that switch resistance does not dominate settling speed is to enforce $R_{on} \ll 1/G_m$ where G_m is the transconductance of the amplifier that contributes to the speed. To reduce the dependence of injected charge on the signal voltage, switches and clock patterns are configured such that injection occurs into the virtual ground (node with stable voltage due to feedback) of an amplifier [102]. A final technique implements half-sized dummy-switches (transistors with source and drain terminals connected as shown in Figure 3.6) placed at the drain and source of the switch and driven by the complement of the switch control signal to nullify the injected charge.

The effectiveness of half-sized dummy-switches relies upon equal partition of the injected channel charge between the source and drain. The partition of charge depends upon the capacitance at the source and drain nodes and also on the transition time of the gate control voltage (ϕ in Figure 3.6) in relation to the time for carriers to transit the channel. Expressions for channel charge partitioning are presented fully in reference [103]. An equal split of injected channel charge is achieved if the capacitances at the source and drain nodes are equal

[2]Throughout this dissertation, the four CMOS transistor terminals: gate, source, drain, and body will be abbreviated as G, S, D, and B, respectively. A voltage with two-terminals in the subscript refers to the potential difference between those two terminals. For example, V_{GS}, is the voltage between the gate and source.

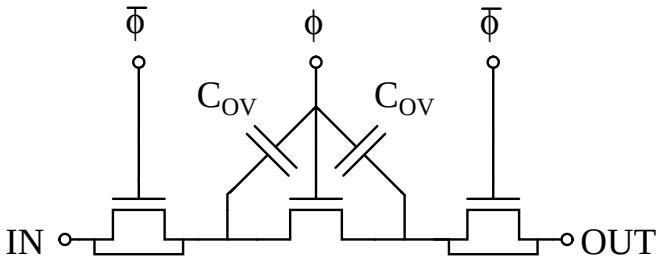


Figure 3.6: An NMOS transistor switch with dummy devices to reduce injected charge. The center transistor is twice as large as the dummy devices on the left and right. The overlap capacitance (C_{OV}) between the gate and drain and gate and source is explicitly shown for the center transistor. ϕ is the switch control signal and $\overline{\phi}$ is its complement.

or if the gate control voltage transitions quickly with respect to carrier channel transit times. For slow transitions of the gate control signal the charge is partitioned relative to the capacitance at each node. Half-sized dummy-switches will not eliminate charge injection entirely due to the complex relation between charge partitioning and circuit parameters. For PAD designs sharp clock edges are the most practical approach to equally split the injected charge and make half-sized dummy switches effective.

Time-of-flight accumulating imagers have implemented fully-differential switched capacitor integrator storage stages so that spurious charge injection is nullified since it effects both output paths equally [98, 104]. However, experimental results have found that layout asymmetries limit the effectiveness of this approach. In reference [104] slight variations of the layout dramatically altered the charge injected per accumulation. One pixel architecture accumulated 1024 times with minor issues from charge injection however, a second pixel architecture was limited to 16 before the output saturated. These results emphasize the subtle significance of layout when spurious charge injection must be minimized. PAD designs may benefit from a fully-differential sampling stage, but such a design has not been implemented due to the increased complexity, area,

and power consumption.

The approach of Figure 3.4 with accumulation at the back-end of the pixel requires slewing and settling of two amplifiers during each sampling period, but decouples the charge-to-voltage gain and full-well of the pixel from the thermal noise added to the signal during each accumulation. The approach with accumulation at the front-end (Figure 4.5) requires the slewing and settling of only one amplifier during each sampling period but charge-to-voltage gain and full-well of the pixel are linked to the thermal noise during each accumulation. Experiments described and discussed in Section 3.5.1 will determine which pixel architecture is most appropriate for the desired detector characteristics.

3.2.3.2 Transistor switch leakage

Transistor switches must hold charge stored on capacitors for the circuits described to work. The transistor switches, however, leak current which corrupts the stored charge. The leakage current arises from two separate mechanisms. The first is subthreshold conduction with exponential dependence on the difference between the gate-source voltage and the transistor threshold voltage. A simplified expression for the drain-source current in subthreshold with $V_{GS} - V_{TH} < -100\,\text{mV}$ and $V_{DS} > 100\,\text{mV}$ is written as:

$$I_{DS} = I_s \frac{W}{L} \exp\left[((V_{GS} - V_{TH})/(nV_t))\right]. \tag{3.23}$$

V_t is the thermal voltage, $I_s = 2n\mu C_{ox} V_t^2$ is the transistor specific current [96] with μ the carrier mobility, V_{TH} is the threshold voltage of the transistor, the body is assumed grounded, and n is the reciprocal slope factor. At room temperature the specific current for an NMOS device in TSMC 0.25 μm CMOS technology is calculated as 325 nA and 70 nA for thick-oxide NMOS and PMOS devices, respectively. For an NMOS switch used in the fabricated prototype with

$V_{GS} = -150\,\text{mV}$ the subthreshold leakage at room temperature from equation 3.23 is calculated as $I_{DS} = 6.7\,\text{fA}$.

The second source of leakage current is reversed-biased junction diodes between the source and drain diffusions and the substrate. The drain diode leakage current is given as [105]:

$$I_{DB} = -I_o(e^{-V_{DB}/V_t} - 1), \tag{3.24}$$

where I_o is the diode saturation current. The diode saturation current depends upon the size of the junction. For a CMOS technology similar to the one used in this work the saturation current per junction area was reported as $0.02\,\text{fA}/\mu\text{m}^2$ at room temperature [106]. Given the diffusion area of PAD transistor switches used the diode saturation current is anticipated to be around 0.02 fA. The leakage from reversed-biased junction diodes will not be significant.

The detector readout-time determines the required capacitor hold-time and should be minimized to limit corruption from leakage. A readout-time of 10 ms bounds anticipated leakage to the level of one x-ray at room temperature (for a bias of $V_{GS} = -150\,\text{mV}$). Subthreshold switch leakage effects can be reduced below the above calculation by careful consideration of node voltages during holding (reduction of switch V_{GS}) and by detector cooling. Later in this chapter leakage measurements for the front-end accumulation circuit are presented. In chapter five, with an apparatus that allows for cooling of the chip, the leakage currents of the storage elements are measured at different stored voltages, temperatures, and levels of x-ray exposure.

3.3 Class AB amplifier

PADs are often built from a mosaic of multiple CMOS ASICs. To increase the contiguous imaging area of the detector wire-bonds are typically confined to a single-side of the die (making a three-side buttable device) and dies are designed to fill the stepper reticle (20 mm × 20 mm). To reduce leakage current from the detector layer analog PADs generally operate at temperatures around -20 °C. These approaches place challenges upon power dissipation in addition to power and ground distribution within the CMOS readout ASIC. Past experience suggests a power limit of 100 μW/pixel.

A class AB amplifier has been incorporated to enhance current provided to the load in a slewing situation without an increase in quiescent power consumption. The class AB amplifier, shown in Figure 3.7, is based on work by Carvajal and colleagues [107, 108].

Transistor groups $\mathrm{M0_{FA}}, \mathrm{M1_{FA}}, \mathrm{M2_{FA}}$ and $\mathrm{M0_{FB}}, \mathrm{M1_{FB}}, \mathrm{M2_{FB}}$ form a flipped voltage follower that presents a low-impedance level-shifted version of the input voltage to the sources of the opposite input transistor (M1, M2) and acts as an adaptive bias. Since a copy of the opposite input voltage is applied to the source of the input devices the effective transconductance of the amplifier is $g_m = 2g_{m1} = 2g_{m2}$, where g_{m1} and g_{m2} are the transconductances of devices M1 and M2 respectively.

A level-shifted copy of the opposite input voltage is presented to the source of each device of the differential pair. This produces a differential current at the input devices proportional to the square of the applied voltage difference. To show this, the current in saturation through $M1$ and $M2$ of Figure 3.7 is written as

$$I_{D1} = \frac{\beta_1}{2}(V_{S1} - V_{G1} - V_{THP})^2, \tag{3.25}$$

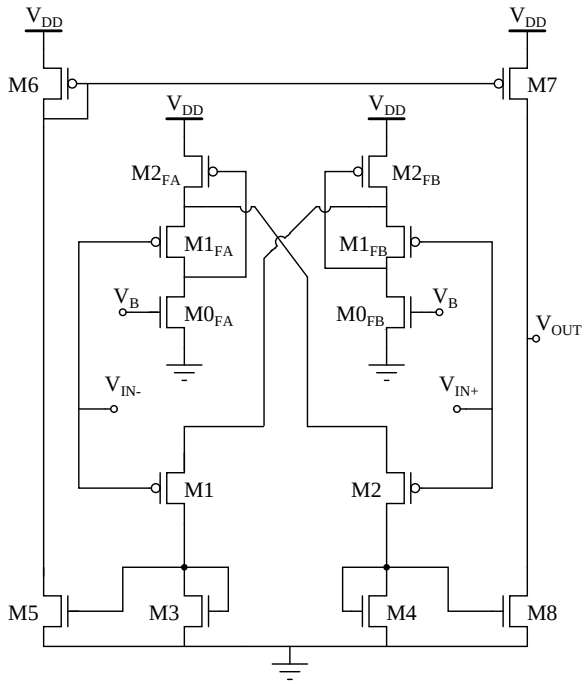


Figure 3.7: Class AB amplifier schematic showing the active bias circuit based on the flipped-voltage follower (transistors $M0_{FA}, M1_{FA}, M2_{FA}$ and $M0_{FB}, M1_{FB}, M2_{FB}$) coupled to a standard current-mirror operational transconductance amplifier. The diode connection at the gates of M3 and M4 may be removed and the drains of M1/M3 and M2/M4 resistively coupled to a node that connects the gates of M3 and M4 for larger current gain.

$$I_{D2} = \frac{\beta_2}{2}(V_{S2} - V_{G2} - V_{THP})^2, \tag{3.26}$$

where I_{DN} represents the drain current of transistor MN, V_{THP} is the threshold voltage of a PMOS transistor, and β_N is the product of the mobility (μ), gate-oxide capacitance (C_{OX}) and transistor strength ratio (W/L) for transistor MN, $\beta_N = \mu C_{OX}(W/L)_N$. The current through $M1_{FA}$ is fixed at the static bias, I_B, through the current source $M0_{FA}$. This sets the voltage at the source of $M1$ and $M1_{FB}$ at $V_{S1} = \sqrt{2I_B/\beta_{1,2}} + V_{IN+} + V_{THP}$. This expression inserted into equation 3.25 gives,

$$I_{D1} = \frac{\beta_{1,2}}{2}(\sqrt{2I_B/\beta_{1,2}} + V_{IN+} - V_{IN-})^2 = \frac{\beta_{1,2}}{2}(\sqrt{2I_B/\beta_{1,2}} + V_{diff})^2, \tag{3.27}$$

where $M1$, $M2$, $M1_{FA}$ and $M1_{FB}$ are equally sized, $\beta_{1,2} = \beta_1 = \beta_2 = \beta_{1F(A,B)}$, and $V_{diff} = V_{IN+} - V_{IN-}$. Similarly, the equation for the drain current of M2 is found as [108]:

$$I_{D2} = \frac{\beta_{1,2}}{2}(\sqrt{2I_B/\beta_{1,2}} + V_{IN-} - V_{IN+})^2 = \frac{\beta_{1,2}}{2}(\sqrt{2I_B/\beta_{1,2}} - V_{diff})^2. \tag{3.28}$$

At large differential input voltages one transistor is turned off and the current difference, $I_{diff} = I_{D1} - I_{D2}$ depends on the square of the voltage difference. Equations 3.27 and 3.28 show that the differential current is not bound by the static bias current I_B.

3.3.1 Flipped voltage follower

The level-shifting element, shown in Figure 3.8, was developed and named a flipped voltage follower (FVF) by Carvajal, et al. [107]. The characteristics of the FVF element, including the DC operating points, the small-signal response, and the stability are presented. A negative feedback loop within the FVF requires its stability as a stand-alone element to be ensured.

In reference to Figure 3.8, consider the biasing of the FVF with no output current and with transistors M1 and M2 in saturation. Saturation of transistor M2 implies $V_{DSM2} > V_{GSM2} - V_{THP}$. Since $V_{SDM2} = V_{DD} - V_{SM1}$ and the voltage at the source of M1 may be written in terms of the quiescent current, I_B, as $V_{SM1} = \sqrt{2I_B/\beta_1} + V_{IN} + V_{THP}$ it is given that

$$V_{DD} - V_{IN} > V_{THP} + \sqrt{\frac{2I_B}{\beta_1}} + \sqrt{\frac{2I_B}{\beta_2}}. \tag{3.29}$$

With similar techniques saturation of transistor M1 gives

$$V_{DD} - V_{in} < 2V_{THP} + \sqrt{\frac{2I_B}{\beta_2}}. \tag{3.30}$$

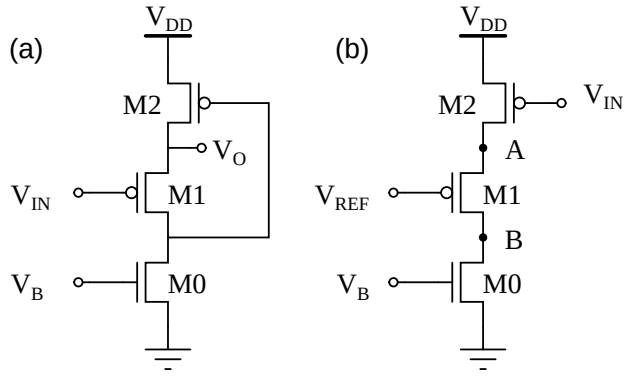


Figure 3.8: Schematic of the three transistor flipped-voltage follower configured with feedback and open-loop. (a) is the schematic of the flipped voltage follower used to level shift the input voltages. The output is taken at node V_O and V_B is the bias of the current source. (b) shows the configuration for open-loop calculations; the connection between the gate of M2 and the drain of M0 is broken, the gate of M1 is given a stable voltage (V_{REF}), the input is applied to the gate of M2, and the output is measured at the drain of M0, node B.

The open-loop gain is given as $A_{open} = -g_{M2}R_B$, where R_B is the open-loop resistance at node B. The impedance at node B is that of the current source M0, r_{o0}, in parallel with the output impedance of the cascode element formed by M1 and M2, $[1 + (g_{m1} + g_{mb2})r_{o1}]r_{o2} + r_{o1}$ [109]. which evaluates to $R_B \approx r_{o0} \parallel g_{m1}r_{o1}r_{o2} \approx r_{o0}$.

The FVF has poles at nodes A and B. The impedance at node A is proportional to the inverse of the transconductance of M1, which is smaller than the impedance at node B. As such, the high-frequency pole is found at node A. The impedance at node A is equivalent to the input impedance of a common-gate stage given as $(r_{o1} + r_{o0})/(1 + (g_{m1} + g_{mb1})r_{o1})$ in parallel with the output impedance of transistor M2 which gives $R_A \approx (1 + r_{o0}/r_{o1})(1/(g_{m1} + g_{mb1})) \parallel r_{o2}$. The capacitance at node B reduces the impedance at node A at high frequencies making it difficult to assign a value to the pole at node A [109].

For an amplifier with a dominant pole the gain-bandwidth product may be

written as $GB = -A_{open}/\omega_{p1}$ where $p1$ is the dominant pole [102]. The dominant pole at node B is given as $\omega_{p1} = \omega_B = 1/(R_B C_B) \approx 1/(r_{o0} C_B)$ and gives a gain bandwidth of $GB = g_{m2}/C_B$. The phase-margin is given as $PM = 90° - \arctan(GB/\omega_A) = 90° - \arctan((g_{m2} R_A C_A)/C_B)$ [102]. To ensure stability the capacitance at node B may be increased. Simulations showed 50 fF at the drain of M0 to be sufficient compensation for stability of the FVF.

To consider the voltage gain from input to output of Figure 3.8 (a) M0 is approximated as a perfect current source ($r_{o0} \to \infty$). The closed loop resistance at the output is given as the open-loop resistance at node A divided by one plus the loop gain:

$$R_{closedOUT} = \frac{R_A}{1 + A_{open}} \approx \frac{1}{g_{m1} g_{m2} r_{o1}}, \tag{3.31}$$

for the case of M0 as a perfect current source. The transconductance is calculated as

$$G_m = \left. \frac{\partial I_{OUT}}{\partial V_{IN}} \right|_{V_{OUT}=0}. \tag{3.32}$$

The transconductance is the product of the gain from V_{IN} to the drain of M1 $g_{m1} r_{o1}$ and the transconductance of M2 which gives

$$G_m = g_{m1} r_{o1} g_{m2}. \tag{3.33}$$

The product of the closed-loop output impedance and the transconductance gives a voltage gain from FVF input to output of approximately one. Hence, the small-signal voltage at the gate of the transistors in the input differential pair is applied without attenuation to the source of the opposite input transistor. This doubles the differential pair transconductance of the class AB amplifier to $G_m = 2 g_{m1}$.

The output impedance of the class AB amplifier is the parallel combination of the output impedance of devices M7 and M8 given by, $R_{OUT} = r_{o7} \parallel r_{o8}$.

The small-signal gain may be increased by lengthening the output loads, M7 and M8, to enhance the output resistance at the cost of output swing. The small-signal differential voltage gain of the class AB amplifier is given as $A_v = 2g_{m1}(r_{o7} \parallel r_{o8}) = G_m(r_{o7} \parallel r_{o8})$. With a 2 μA bias for each FVF element the voltage gain was simulated to be around 500 V/V or 54 dB. This architecture does allow cascoding at the output branch for increased voltage gain. However, output voltage swing and reduced complexity was preferred over high voltage gain.

3.4 Design tool: amplifier testbench

For efficient amplifier design a simulation testbench was developed to extract the dependence of amplifier performance metrics on relevant circuit parameters. Inserted into the testbench is a SPICE [110, 111] file of the amplifier under-test (DUT) with required names for the input and output nodes (shown in Figure 3.9). The testbench SPICE files establish all necessary biases, load capacitances, supply voltages, test sources, and measurement points. When an amplifier is modified the testbench files do not change. The testbench software evokes T-SPICE [112] from the Windows command-line to execute simulations in an automated fashion and parses the output to populate *Matlab* (The MathWorks Inc., Natick, MA, USA) arrays for analysis and plotting. This software was developed to emphasize that amplifier performance metrics are not fixed but are closely linked to various circuit parameters. Understanding these dependencies is critical to PAD design.[3]

An example result from the AC testbench is shown in Figure 3.10, which plots the amplifier transconductance versus current from the supply for four different amplifiers. The transconductance ratio, G_m/I_{tot}, is around $5\,\mathrm{V}^{-1}$ at low

[3]Appendix computer file pointer for test-bench: TB1

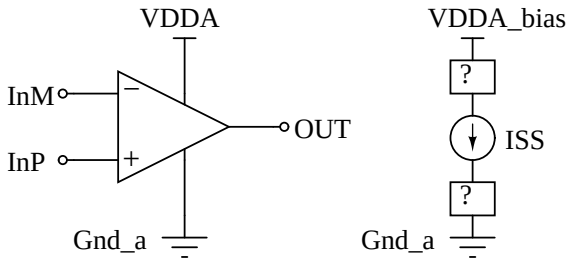


Figure 3.9: The required format of the amplifier under-test (DUT). The SPICE file requires the nodes VDDA, Gnd_a, OUT, InP, and InM. The current source and ? labeled boxes on the right represent the bias network of the amplifier. The bias of the current source is represented by ISS which is a parameter for modification by the testbench. The bias network is powered from a supply (VDDA_bias) different from the main amplifier so that the power draw of the bias network is not counted toward the power consumption of the amplifier.

current levels and falls to around $2\,\mathrm{V}^{-1}$ at higher current levels. The 'NMOS FC.' amplifier G_m versus I_{tot} remains linear for larger currents because the input devices are wider and are biased closer to subthreshold for a given current draw than the input devices of the other amplifiers. In strong inversion the transconductance of NMOS devices is around a factor of five greater than equally-sized PMOS devices with equal drain current due to the larger mobility of electrons. Figure 3.10 shows that, since PAD devices operate closer to weak-inversion, the superior transconductance of NMOS devices is not fully realized.

An example from the slew-rate testbench is shown in Figure 3.11. The amplifiers are configured at equal current dissipated and the current to the load is plotted versus the voltage difference, V_{DIFF}, between the input nodes.

Tables 3.1 and 3.2 list the SPICE files and *Matlab* functions that are part of the testbench software.

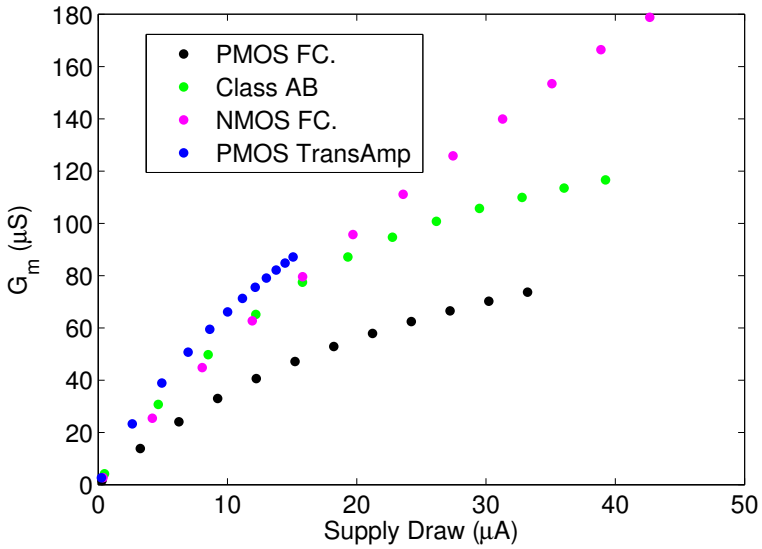


Figure 3.10: An example of results from the amplifier testbench software. The transconductance is extracted as a function of the total current drawn from the power supply for four different amplifiers. 'PMOS FC.' is a folded cascode differential amplifier with PMOS input devices and a low dropout current mirror. 'Class AB' is an amplifier that will be described in detail in a later section. 'NMOS FC.' is the same architecture as 'PMOS FC.' but with transistor types swapped so that the input devices are PMOS. 'PMOS TransAmp'is a five transistor differential amplifier with current mirror loads and PMOS input devices.

Table 3.1: Indicates the file names of the SPICE testbenches developed and lists the variable parameters and measurement results of each.

File	**Parameters**	**Measurements**
OpenLoopGain_TB.sp	integrated charge, V_{REF}, bias current, load capacitance	unity-gain freq., max-gain, phase-margin, supply draw, transconductance, input capacitance
SlewRate_TB.sp	differential input voltage, bias current,	current to load
Noise_TB.sp	bias current, load capacitance	output PSD (V/ $\sqrt{\text{Hz}}$), integrated output noise (V)

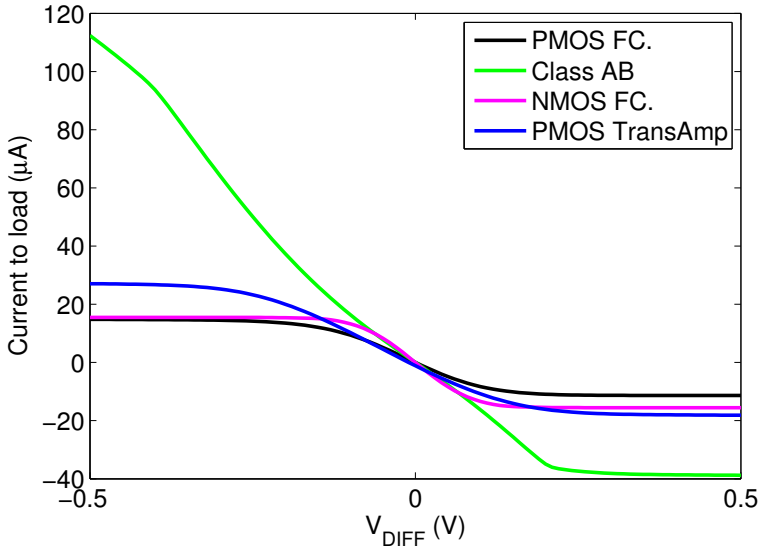


Figure 3.11: Current supplied to the load for the amplifiers described in the caption of Figure 3.10 versus V_{DIFF}. The total supply draw for each amplifier was measured to be 30 μA. The amplifier inverting input and output voltage is elevated above V_{REF} by the value of V_{DIFF}. The non-inverting input terminal is held at V_{REF}.

Table 3.2: *Matlab* functions that evoke the SPICE testbenches, parse the results, and plot the data.

Function: (Purpose)	**Input**	**Output**
opAmpTestBench.m: (runs simulations and populates data arrays)	amplifier SPICE file name	parameters and data from ac, slew-rate, and noise analysis
plotACresults.m: (plots ac data results versus one parameter while holding other parameters constant)	parameter and data to plot, data and parameter values and names	plot and handle to plot
ReadACopenloop.m: (extracts AC measurements)	name of SPICE output file	AC parameters and data
ReadSlewRate.m: (extracts slew-rate measurements)	name of SPICE output file	slew-rate parameters and data
ReadNoise.m: (extracts noise measurements)	name of SPICE output file	noise parameters and data
Edit_DUTrad.m: (modifies DUT spice-file to add threshold shifts)	name of DUT SPICE file to modify	DUT file with voltage source of value VTHN and VTHP at each NMOS and PMOS gate
unique_param_val.m: (displays values and indices of parameters)	parameter name to display (or 'all'), parameter values and names	parameter values and indices

3.5 Test chip one

3.5.1 Instrumentation

3.5.1.1 Prototype ASIC

A prototype ASIC was fabricated through MOSIS in TSMC mixed-mode, non-epitaxial substrate 0.25 μm CMOS process using thick-oxide 3.3 V transistors.[4] The purpose of the chip was to confirm the functionality of the circuits for accumulation and to compare the speed of different amplifier architectures. The chip, shown in Figure 3.12, included two individually addressable 6×8 pixel arrays. One of the 6×8 arrays contained pixels as shown in Figure 3.4; the other array held pixels as shown in Figure 4.5. Pixels in this prototype measured $\simeq 100\,\mu\text{m} \times 100\,\mu\text{m}$. Each 6×8 (rows $\times$ columns) pixel array had an eight-to-one analog multiplexer that buffered the selected pixel output to a dedicated wire-bond pad.

The analog multiplexing and row selection was controlled by two bit-passing shift registers. The shift registers were built from NAND-based D flip-flops with asynchronous clear and preset. NMOS transistors in the flip-flop were drawn as enclosed layout devices and n+ diffusions at different potentials were guarded.

Pixel monitoring was available through probe-pads at the front-end output and the pixel output (FE_{OUT} and PIX_{OUT}, respectively in Figures 3.4 and 4.5) and the pixel output in four pixels per array. Three columns in each array had a 6.24 μm^2 charge injection MOS capacitor extracted as 195 fF at the pixel inputs, and three columns had a $0.72{\times}0.36\,\mu\text{m}^2$ charge injecting MOS capacitor ex-

[4] Appendix computer file pointer for schematic: SchP1, appendix computer file pointer for layout: LP1, appendix computer file pointer for simulations: SimP1.

tracted as 6 fF. One column has a high-bandwidth p+/n+ photodiode explained in the dissertation of Li [113]. This photodiode design, compatible with standard CMOS processing, places interdigitated p+ and n+ fingers in an n-well to allow for collection via carrier drift.

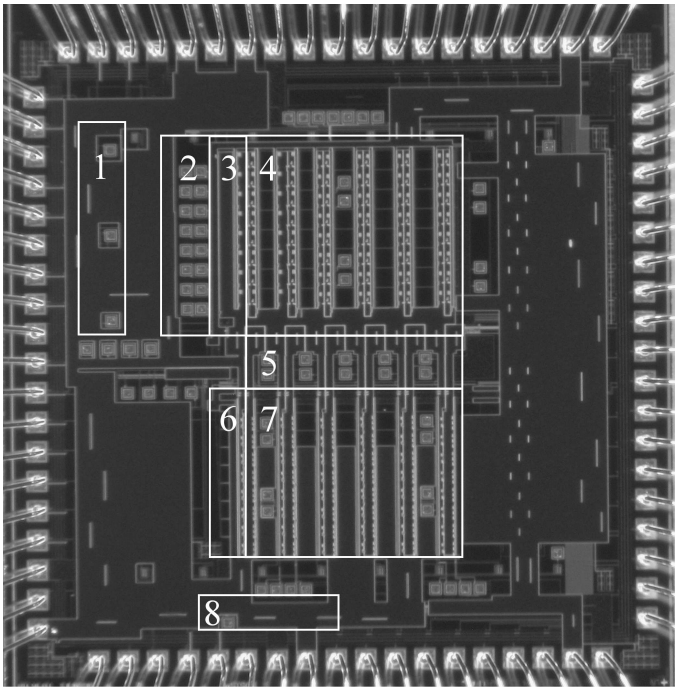


Figure 3.12: A microphotograph of the prototype chip. The chip measured 3.3 mm × 3.3 mm. The labeled areas are as follows: 1) amplifier test structures, 2) column addressing register, 3) front-end accumulation array output multiplexer, 4) 6 × 8 front-end accumulation pixel array, 5) row addressing register, 6) back-end accumulation array output multiplexer, 7) 6 × 8 back-end accumulation array, 8) MOS transistor R-2R current-splitter.

The test chip explored performance differences between two folded cascode amplifiers with a low-voltage cascode current mirror, one with NMOS input devices and a second with PMOS input devices, and the described class AB amplifier. This low dropout folded-cascode architecture allows for a large voltage swing at the output. The bias network, which is critical to proper operation of this amplifier, was based on a cascode bias network designed for all current lev-

els presented by Minch in reference [114]. Each amplifier design is used in two rows of both arrays. The chip also contains isolated amplifier test structures of all three types. Each amplifier test structure output is available at a wire-bond pad and a probe-pad.

All NMOS transistors within the test chip are designed using radiation hardened layout techniques: transistors with large width-to-length ratios are drawn using enclosed layout techniques [115] while transistors with smaller width-to-length ratios are drawn using a radiation hardened linear technique that dopes the edges of the polysilicon gate p-type to increase the threshold voltage of radiation-induced parasitic edge transistors [116]. Where a reduction in charge-injection is necessary to limit spurious signal during accumulation switches use a half-sized dummy switch driven by an inverted clock signal. Simple non-overlapping clock generators are used to control the switches in the sampling stage of Figure 3.4 to minimize the time when the amplifier is configured without feedback. A radiation hardened version of the MOS transistor R-2R current-splitter, designed by Delbruck and van Schaik to digitally control bias currents and voltages on chip, was implemented as a test structure and confirmed functional [117]. For this prototype, arrays of storage capacitors were limited to four elements for simplicity and a reduction of wire-bond count.

3.5.1.2 Support electronics

The chip was packaged in a pin grid array (PGA) carrier (MOSIS package name PGA108M) and mounted to a printed circuit board (PCB)[5] via a zero-insertion-force (ZIF) socket. Bias currents and reference voltages were set by 100 kΩ digital potentiometers (Microchip technology, MCP42100-I/ST) on the PCB. The potentiometers were programmed via the SPI protocol using the Aardvark

[5]Appendix computer file pointer for printed circuit board: PcbP1.

I2C/SPI host adapter from Total Phase (Sunnyvale, CA). Digital control signals to the ASIC were created by a 32 channel PI-2005 pattern generator from Pulse Instruments (Torrance, CA). The pattern generator was connected to the PCB with four 8W8 D-subminiature connectors ordered from Conec (Garner, NC, model 3008W8SXX78N20X). These connectors are D-Subminiature with eight coaxial contacts per connector. Base digital patterns were designed in the graphical PI-PAT software distributed with the pattern generator. The base patterns were exported to text files and executed via the command-line interface to the pattern generator executable. Data was acquired using an oscilloscope (Agilent Technologies, Santa Clara, CA, model MSO6054A). Test-pads were monitored using both a standard 12C picoprobe (1 MΩ input resistance) and, when the current-drive of the circuit under test was limited, a high-input impedance (input leakage 10 fA) 18C picoprobe (GBB Industries Inc., Naples FL). All experiments were performed with the chip in a light-tight enclosure at room temperature.

3.5.2 Experiments and results

3.5.2.1 Accumulation

Accumulation functionality was verified for both pixel varieties. The concept is illustrated in Figure 3.13. The sequence of steps is delineated by dashed vertical lines and proceeds as follows:

1. Pixel reset: x-ray signal is shuttered.
2. Accumulate three injection pulses onto frame 1 (F1).
3. Pixel reset: x-ray signal is shuttered.
4. Accumulate one injection pulse onto frame 2 (F2).

5. Pixel reset: x-ray signal is shuttered.
6. Re-address frame 1 (F1) and recover voltage stored at the conclusion of step 2 (at 5 μs). Accumulate three injection pulses onto frame 1. Frame 1 now holds the sum of the signal from step 2 and step 6 which equals six charge injection operations.
7. Pixel reset: x-ray signal is shuttered.
8. Re-address frame 2 (F2) and recover voltage stored at the conclusion of step 4 (at 10 μs). Accumulate one injection pulse onto frame 2. Frame 2 now holds the sum of the signal from step 4 and step 8 which equals two charge injection operations.

This architecture may also switch immediately between frames without intermediary shuttering of the x-ray signal.

An injected signal of 6 mV per accumulation was measured for the switched capacitor architecture due to charge injection and finite amplifier gain. Circuit non-idealities saturate the pixel in approximately 100 accumulation operations. Fully-differential sampling architectures would reduce spurious signal due to charge injection [98]; however, the area and power costs need to be explored and may be prohibitive. The injected signal per accumulation was measured to be 500 μV for the front-end accumulation architecture. This architecture was found to reach an equilibrium where dark accumulations no longer inject spurious signal, thus allowing further accumulations without pixel saturation.

3.5.2.2 Settling time

Pixel settling time was studied by varying the time between charge injection into the pixel input and the sampling of the front-end output by the storage stage. The value held by the pixel was then read out through the analog output

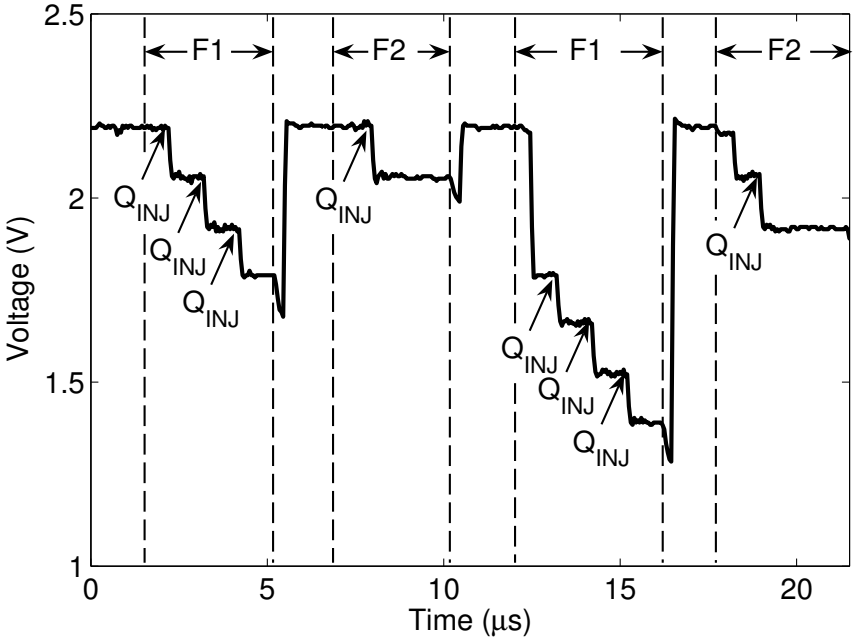


Figure 3.13: Oscilloscope trace taken at node FE_{OUT} of Figure 4.5 using a pico-probe that displays the accumulation function in the pixel. At each point indicated by Q_{INJ} a charge of 70 fC, equivalent to 200 x-rays (8 keV), is injected into the front-end. The regions labeled 'F1' and 'F2' indicate respectively, acquisition onto the first frame element (C_{F1} in Figure 4.5) and acquisition onto the second frame element (C_{F2} in Figure 4.5). The second 'F1' and 'F2' regions begin at the voltage reached at the conclusion of the first region thus displaying the accumulation functionality.

chain. The output voltage measured is plotted versus the time between charge injection and sampling in Figure 3.14(a). The results are shown for each amplifier configured at a static power consumption of 43 μW. Results were measured to be similar for the front-end accumulation architecture except for anticipated differences due to changes in loading capacitance. The class AB amplifier at a power dissipation of 43 μW slews the equivalent of 685 8 keV x-rays in less than 40 ns whereas the folded-cascode amplifiers require 100 ns. Figure 3.14(b) shows the small-signal approach to the final value. The overshoot at 50 ns of the class AB amplifier reveals a deficient phase margin which will be adjusted in future fabrications. The slew-rate of the folded cascode amplifiers is calculated

from (3.12) (with an adjustment for the loading of the injection capacitor) to be 1.1×10^7 V/s whereas 8.8×10^6 V/s is measured. The deviation is anticipated to be due to parasitic capacitance within the pixels. Another possible cause for the discrepancy is that the amplifiers supply less than half of the total bias current to the load during slewing (measured at $\approx 85\%$ by simulation). Isolated class AB amplifier test structures configured in unity-gain and operated at 53 μW dissipation were found to drive larger load capacitances with a current of $I_{load} = 26I_{tot}$ and $I_{load} = 24I_{tot}$ for falling and rising slew operations respectively.

3.5.2.3 Noise

The fixed read noise and noise per accumulation was measured for both architectures and is shown in Figs. 3.15 and 3.16. The noise was found to have limited dependance upon amplifier architecture but was greatest for the class AB amplifier. The noise power per accumulation was around twice as large for the back-end accumulation architecture because of the larger number of sampling events per accumulation for this architecture. The noise dependence on the input capacitance was studied by placing an explicit load capacitor of 195 fF at the pixel input. As is seen in Figure 3.16 the growth of the equivalent noise charge (ENC) power per accumulation was measured to be $(572\,\mathrm{e}^-)^2$ and $(413\,\mathrm{e}^-)^2$ with and without an explicit capacitive input load respectively. A hybridized detector layer is anticipated to introduce a smaller capacitance, 130 fF, than the explicit test load, 190 fF.

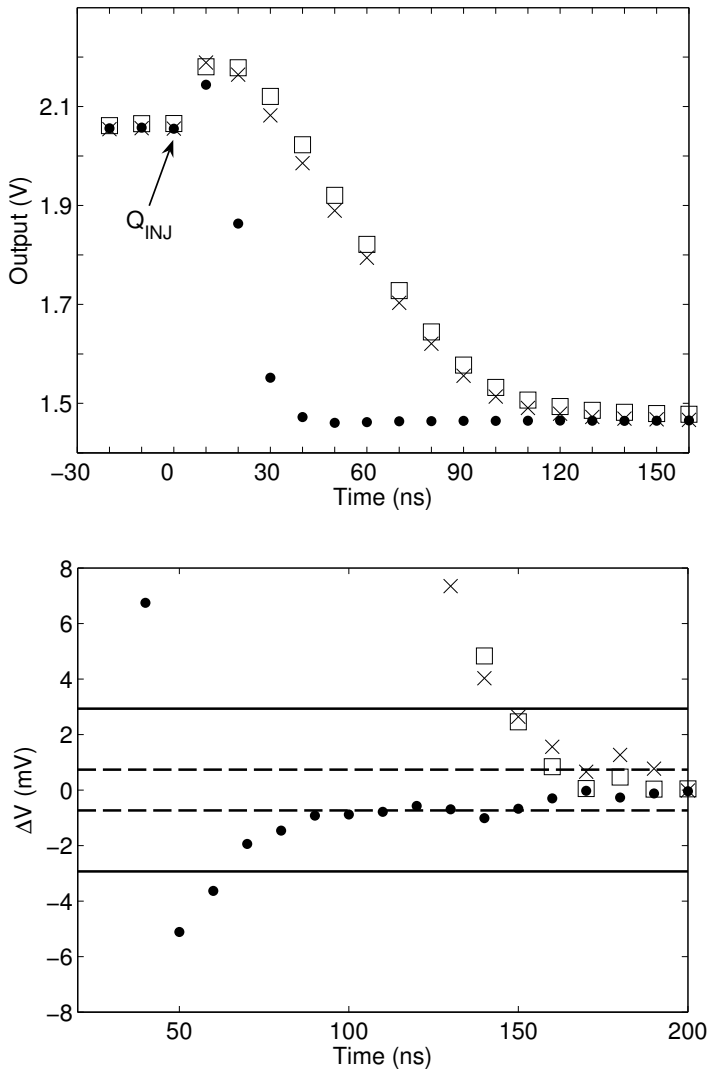


Figure 3.14: (a) Comparison of front-end output slewing following injection of charge for the class AB amplifier (•), the NMOS input folded-cascode (×), and the PMOS input folded-cascode (□) at equal quiescent power dissipation of 43 μW. At $t = 0$ ns a charge of 240 fC, equivalent to 685 x-rays (8 keV), is injected into the front-end. (b) Small signal settling calculated from the data shown in (a). Plotted is the deviation (ΔV) from the final settled value versus delay time. The solid line indicates 8-bit accuracy given a 1.5 V range while the dotted line indicates 10-bit accuracy.

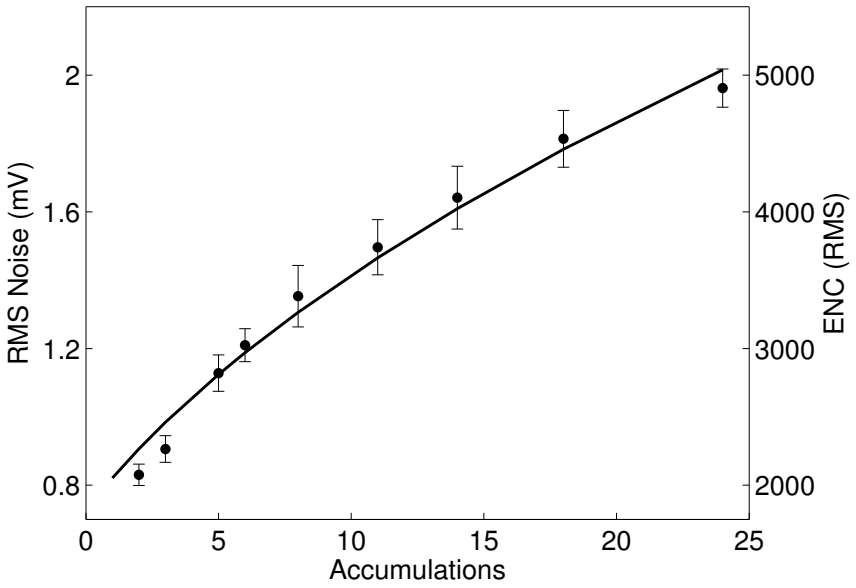


Figure 3.15: Noise growth versus accumulations for the back-end accumulating pixel configuration using the class AB amplifier at both the front-end and the sampling-stage. A fit to the data (solid line) returns $\sigma^2 = (726\,\mu\mathrm{V})^2 + (384\,\mu\mathrm{V})^2 N$; $\sigma^2 = (1815\,\mathrm{e}^-)^2 + (960\,\mathrm{e}^-)^2 N$ with N the number of accumulations. Error-bars represent the standard deviation of the noise measured between seven different pixels in the column.

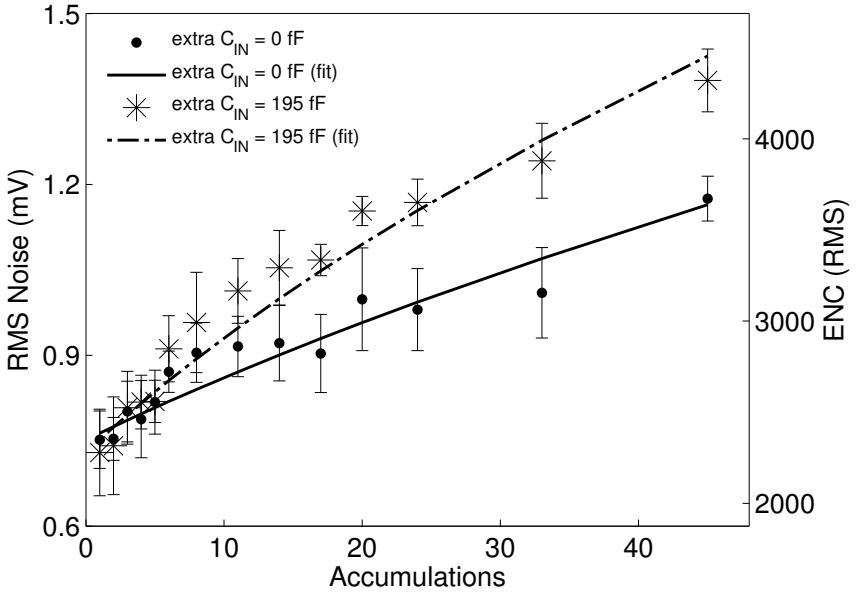


Figure 3.16: Noise growth versus accumulations for the front-end accumulating architecture using the class AB amplifier at the front-end. Measurements from pixels with an extra input capacitive load of 195 fF ($*$) and pixels without an explicit loading capacitance ($\bullet$). Fits to the data return $\sigma^2 = (752\,\mu\text{V})^2 + (132\,\mu\text{V})^2 N$; $\sigma^2 = (2350\,\text{e}^-)^2 + (413\,\text{e}^-)^2 N$ (solid red line) and $\sigma^2 = (729\,\mu\text{V})^2 + (183\,\mu\text{V})^2 N$; $\sigma^2 = (2278\,\text{e}^-)^2 + (572\,\text{e}^{-2}) N$ (dashed-dotted line) with N the number of accumulations and the constant read-noise term taken from the measurement. Error-bars represent the standard deviation of the noise measured between eight different pixels without explicit capacitive load and six pixels with additional capacitive load.

3.5.2.4 Storage element hold times

Storage element hold times were evaluated at the front-end accumulation elements. The charge injection circuit was used to vary the charge stored across C_{F1}, as shown in Figure 4.5. After injecting charge, switch Φ_{F1} was opened (a PMOS transistor), the pixel front-end reset to V_{REF}, and the charge across C_{F1} held for up to 12 s. After the specified hold time the pixel value was read. During a hold operation with the pixel reset to V_{REF} the Φ_{F1} switch source voltage, V_S, is given as $V_S = V_{REF} + Q_{IN}/C_{F1}$. Forward biasing of the transistor source-to-bulk p-n junction limits the maximum V_S to V_{DD}. This limit suggests an optimal V_{REF} of $V_{DD}/2$ to maximize front-end swing without loss of signal through a forward biased p-n junction of switches Φ_{F1-4}. At levels of low injected charge the hold-switch gate-source voltage, V_{GS}, remains below -400 mV, so that the transistor is in accumulation-mode and subthreshold drain-to-source leakage current is minimal [105]. Leakage of 2 fA that increased the charge stored across C_{F1} was measured. When V_{GS} exceeds -200 mV the transistor enters weak inversion and drain-to-source current increases. The maximum leakage current measured was 0.5 fA discharging C_{F1} with $V_{GS} = -80$ mV and $V_{DS} = -1.57$ V. These results suggest that maximum exposure times are limited to seconds by the holding ability of analog storage elements. Further improvement of storage element hold times may not be successful as detector layer leakage (~ 100 fA/pixel) will limit the minimum resolvable x-ray flux. The above measurements were taken with the chip at room temperature. A reduction of leakage currents that corrupt storage elements is anticipated when the detector is cooled. Studies of the hold-times of the storage capacitors, C_{Sn}, will be presented in chapter five, section 5.4.

3.5.2.5 Linearity and cross-talk

Linearity and analog storage element cross-talk were evaluated by independently varying the number of magnitude 9.6 fC charge packets injected into the front-end before storage onto C_{S1} and C_{S2}. Following injection both storage elements were read through the analog output chain. The pixel output for C_{S2} along with a linear fit is plotted versus the total charge injected in Figure 3.17. The relative error of measured data from fit is plotted in the inset and remains below 6×10^{-3} for injected charge up to 660 fC (equivalent to 1880 8 keV x-rays). For this experiment only one C_F capacitor was connected across the front-end amplifier. For flash-mode operation or accumulation onto only a single frame the full-well could be increased fourfold by engaging all C_{F1-4}. The same experiment was used to evaluate cross-talk between the value acquired by each storage element. No cross-talk was observed down to levels below 1 mV.

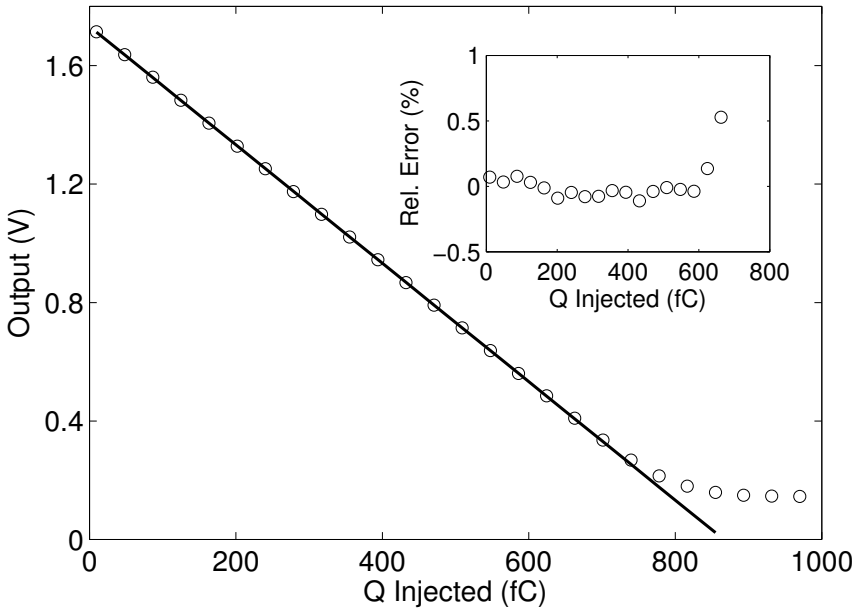


Figure 3.17: Pixel output (∘) and a linear fit (solid-line) plotted versus charge injected. The inset shows the Relative Error (Rel. Err. = (measured-fit)/fit) for injected charge of up to 660 fC.

3.5.2.6 Radiation robustness

X-ray conversion in the SiO_2 of CMOS circuits produces electron-hole pairs that modulate transistor performance. In SiO_2 electrons are sufficiently mobile to escape but holes remain, which leaves a positive fixed oxide charge after x-ray conversion. The voltage produced by the positive gate-oxide charge adds to the gate-bias to effectively shift the threshold voltage of the transistor. The effective threshold shifts negative for NMOS transistors. Studies of TSMC 0.25 μm process have found a -17 mV threshold shift after 2.5 kGy(Si) and -50 mV after 10 kGy(Si) [118][6]. PMOS threshold voltages become more negative. Reference [118] found a shift of around 5 mV for PMOS transistor thresholds. Our designs have utilized the thick-oxide option for supply voltage operation at 3.3 V, whereas reference [118] used standard oxide thickness transistors with a 2.5 V supply voltage. The threshold shifts of thicker oxides are more severe due to a larger cross-section for conversion and lower probability of hole escape by tunneling [119, 120].

Trapped oxide charge also modulates the threshold voltage of parasitic transistor structures along areas covered by field-oxide. Trapped oxide charge builds up rapidly in field-oxide due to its thickness. For example, the threshold voltage of a field-oxide transistor was measured at 42, 31, 11, and 0.46 V after accumulated does of 0, 100, 500, 1000 Gy(Si) [118]. Charge that builds up in the field-oxide may invert p-doped substrate underneath and create a channel between n-diffusions. Due to this susceptibility mechanism NMOS transistors are designed using radiation hardened layout techniques. Transistors with large width-to-length ratios are drawn using enclosed layout techniques [115] so that

[6]The gray (Gy) is 1 joule absorbed per one kilogram of matter. For a given flux of x-rays the absorbed energy depends on the absorbing material so dose levels should be referenced with the material followed in parentheses.

no field-oxide path exists between source and drain. Transistors with smaller width-to-length ratios are drawn using a radiation hardened linear technique that dopes the edges of the polysilicon gate p-type to increase the threshold voltage of radiation-induced parasitic edge transistors [116]. Further, field-oxide paths between n+ or n-wells at different potentials should be guarded by placement of a p+ substrate implant to breakup any parasitic channel formation.

Radiation robustness was evaluated by dosing an electrically biased ASIC at room temperature at a rate of 0.9 Gy(Si)/sec. Dosing used a rotating anode source operated at 40 kV and 50 mA (Enraf Nonius, Model FR571, Bohemia, NY) with multilayers to select 8 keV radiation (Osmic model CMF15-165Cu8, Troy, MI). A 1.3 mm diameter pinhole was visibly aligned with the chip to select an area of dosing. A phosphor surrounding the edges of the pinhole was then used as a guide while directing the x-ray beam through the pinhole.

First, biasing structures were dosed to measure transistor threshold shifts as a function of dose. The current drawn by a diode connected rad-hard linear NMOS device of a multiplicity of 10 with W/L =1.44 μm/0.72 μm was continuously monitored. Simulations were then used to extract the threshold shift that corresponded to the measured drain current. The extracted change in threshold voltage versus time is shown in Figure 3.18.

The threshold voltage shifts in Figure 3.18 are not as dramatic as reference [118]. This emphasizes the effect of the oxide electric field on accumulated damage. The fraction of electron-hole pairs that recombine decreases when the electric field across the oxide is increased [119]. Transistors were biased at standard operating potentials in these experiments and at worst case bias in reference [118], which gives fields of $\simeq$ 1 MV/cm and $\simeq$ 4 MV/cm, respectively. Other possible causes of the difference in threshold voltage change versus accumu-

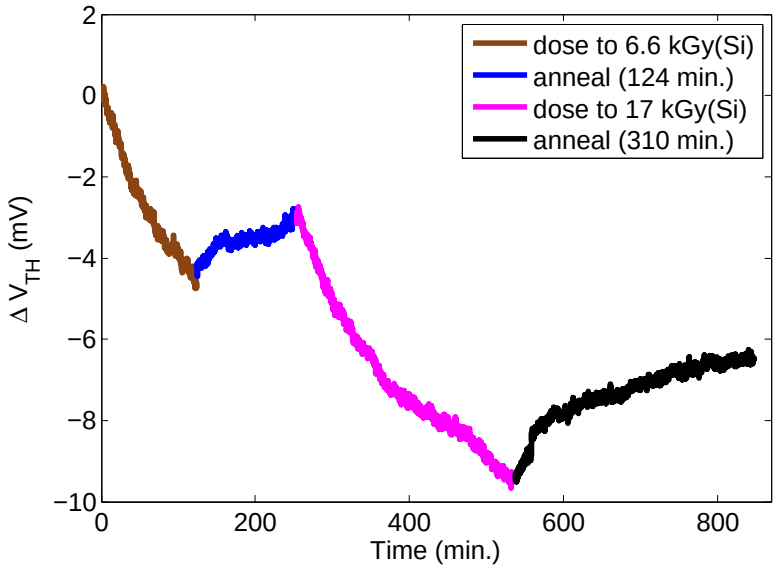


Figure 3.18: Measured NMOS transistor threshold shift during cycles of dosing and annealing.

lated dose include temperature and dose-rate.

The cause of threshold voltage shifts can be partitioned into trapped charge, which can be removed by annealing, and interface state generation, which can not be removed by annealing. Studies of the fraction of the threshold shift due to trapped charge would allow for prediction of the threshold shift after cycles of dosing and annealing.

Next, the x-ray beam was aimed at parts of the pixel array and the addressing registers. After total accumulated dose levels of 10 kGy(Si) and 70 kGy(Si) both falling and rising transitions of the addressing registers were evaluated and the response to injected charge of dosed pixels (similar experiment to Figure 3.17) was studied. Address register functionality was tested with picoprobes at test-pads and remained at each accumulated dose level. No change in edge rise or fall times were detected. At 70 kGy(Si) accumulated dose the readout of the signal due to injected charge was compromised.

Further investigation revealed failure of the NMOS input device folded cas-

code amplifier used to drive the stored value out of the pixel. Picoprobe measurements at pixel output test-pads were used to monitor the output buffer when configured into unity gain. It was found that the output did not exceed a voltage of 400-600 mV as the reference voltage at the non-inverting terminal was raised (both standard and high input impedance picoprobes measured similar results). The output voltage of 600 mV was measured when the amplifier was biased at higher current levels.

The bias voltages of the transistors in this circuit were set aggressively in order to maximize voltage swing; this was a mistake in terms of radiation robustness. In Figure 3.19 the amplifier architecture is shown with the current through the differential pair current source labeled as I_{TAIL} and the current through the PMOS devices that bias the output branch labeled as $I_{O-BRANCH}$. In standard operation the amplifier bias voltages are configured so that $I_{TAIL} = I_{O-BRANCH}$. After radiation damage the current draw is anticipated to increase for the NMOS devices and decrease for the PMOS devices. One possible failure mechanism is an increase of I_{TAIL} to twice $I_{O-BRANCH}$. In this case, no current would remain to drive the output voltage toward V_{DD}.

The mechanism hypothesized above for the experimentally measured amplifier failure was confirmed in simulation using a tool from the amplifier testbench software. *Edit_DUTrad.m* parses a SPICE file and inserts a voltage source at the gate of all transistors within the amplifier in order to emulate radiation induced transistor threshold shifts. The value of the voltage source is given by the parameters VTHN and VTHP at the gates of NMOS and PMOS transistors, respectively. With the created DUT SPICE file the amplifier response versus the change in transistor threshold may be simulated. A shift of -40 mV and -10 mV, for the NMOS and PMOS devices respectively, showed the amplifier to fail to

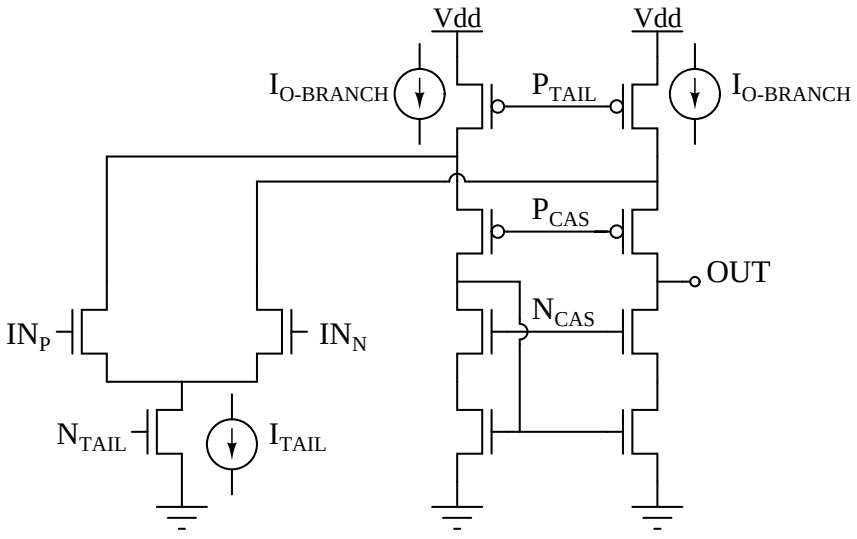


Figure 3.19: Schematic of the NMOS input folded-cascode differential amplifier. The PMOS input folded-cascode used the same architecture but with transistor polarities swapped.

buffer voltages above 800 mV in simulation.

These results call into question the relative amplifier radiation tolerance hierarchy found in chapter 2 of reference [50]. The folded cascode architecture requires relative matching between NMOS current sources and PMOS current sources, which is difficult to maintain after transistor threshold voltage shifts. Since the input differential pair uses PMOS devices, the folded cascode amplifier presented in reference [50] should handle threshold shifts without catastrophic failure. Yet, the slew-rate for rising outputs and speed at constant power dissipated will be reduced as a larger proportion of the current is drawn by the output branch than by the input differential pair. Amplifiers with simple biasing (a single transistor current source) and current-mirrors may be more robust under transistor threshold voltage shifts than amplifier architectures that require multiple bias voltages.

The Class AB amplifier was functional after accumulated dose levels of 70 kGy(Si). A 500 μm thick silicon detector layer will attenuate the dose to the

CMOS by a factor of 1300 with an incident x-ray energy of 8 keV and by 5.6 with an incident energy of 13 keV. For a flux of 1000 x-rays in 100 ns per pixel at 8 keV x-ray energy the CMOS chip receives a dose of 2.6 Gy(Si)/sec. For a radiography experiment at 8 keV at the above flux specification, a 1 ms shutter opening time, and a 100 Hz repetition rate, the measured failure level of 70 kGy(Si) would be reached after 80 hours of data acquistion. Results in chapter five will show improvements in tolerance to x-ray dose after modifications to the ASIC design.

3.6 Conclusion

A prototype ASIC for development of an analog PAD with timing resolution sufficient to isolate single synchrotron bunches has been designed, fabricated, and tested. The pixel has analog memory to store multiple frames so that the time between snapshots is not limited by detector readout. Each frame may be re-addressed and signal added to provide in-situ averaging that may draw low-level signals above the read-noise floor.

Two switched-capacitor pixel architectures were explored to accomplish in-pixel accumulation. One uses a discrete-time integrator at the pixel back-end to allow for re-addressing and addition to storage elements. The other pixel architecture uses the front-end integration capacitors as storage elements during signal acquisition. Both architectures were tested and confirmed functional. The architecture that accumulates at the front-end (Figure 4.5) was measured to have better noise performance, lower spurious signal per accumulation, and a lower power requirement for a given settling time than the architecture that accumulates at the pixel back-end (Figure 3.4).

Timing resolution was shown to be limited by slewing for high-flux signals. To address this issue a class AB amplifier was designed and tested. The class AB

amplifier provides a current to the load greater than the static bias during a slewing event. Experiments showed settling of the equivalent of 650 8 keV x-rays (227 fC) in less than 100 ns.

In terms of 8 keV x-rays the fixed ASIC read-noise was measured to be 1.1 x-rays while the noise was found to grow with the square-root of the number of accumulations at a rate of 0.19 x-rays. An improvement to the fixed detector read-noise without subsequently sacrificing detector full-well is desired. A possible approach to improve the read-noise is to implement digital full-well extension techniques, which would allow an increase in the front-end charge-to-voltage gain without sacrificing full-well [50]. Digital extension techniques remove charge from the front-end integration capacitor and increment an in-pixel counter when the front-end output passes a threshold. At exposure end, the pixel output is the combination of the counter value and an analog residual. However, an extension technique will only be acceptable if the minimum time resolution is not sacrificed.

The detector was found to respond linearly to injected charge of up to 1880 x-rays of 8 keV energy (660 fC) into a single frame element. Unfortunately, only about one-half of the supply voltage is used for signal acquisition due to limited amplifier swings and switches with p-n junctions that forward bias during certain holding configurations. Techniques to increase the supply voltage utilization to raise the saturation value could be pursued. First, switch type and architecture (ie, switches on the sides of both plates of capacitors) should be carefully chosen. Further, since CMOS transistor reliability depends on relative voltages between terminals rather than absolute voltages, over-driving certain switches may expand the usable voltage range of the pixel without risking damage to the transistors [121].

The designed class AB amplifier showed sufficient slew-rate to meet the desired speed requirements and will be pursued with a slight redesign for improved phase margin. The measurements in this chapter showed the pixel architecture that resampled at the front-end feedback capacitors to have lower noise performance per accumulation. Radiation damage measurements showed a need for a redesign of the in-pixel output buffer.

The support electronics for analog output digitization and digital input control signal generation required improvement. Measured noise was generally found to be higher than anticipated calculations, which may be due to the support electronics. Less external noise is desired to help understand the fundamental noise levels of the chip.

The pixel functionality is ultimately set by the flexibility of the control electronics that drive the transistor switches. The flexibility and ease of use of the digital pattern generation needed improvement. Tests at full readout speed require high-speed control electronics and will provide information on the in-pixel output buffering and the column-level analog multiplexing.

For the next phase of this work it was decided to develop a 16×16 pixel readout chip that could be hybridized to detector chips for photon detection. In addition, support electronics would be developed with flexible and robust field-programmable gate array (FPGA) based detector control and readout to create a full imaging system. In all ways, other than the small imaging area, this camera development should mimic a final detector design.

CHAPTER 4

SMALL-AREA CAMERA DEVELOPMENT FOR SINGLE-BUNCH X-RAY IMAGING

4.1 Introduction

This chapter presents the design of a 16×16 pixel camera for x-ray imaging. The design of the CMOS readout chip is explained. The support electronics built around the readout chip, crucial for functionality and for fully realizing the features of the readout chip, are next described. A fundamental portion of the support electronics are the digital control signals sent to the CMOS readout chip by a field programmable gate array (FPGA) device. The state machines implemented in the FPGA via hardware description language code are differentiated into blocks by the stages of the image acquisition sequence that each controls. Software writes via USB to control registers in the FPGA set the fundamental parameters of the image acquisition sequence. The variables that are written to FPGA registers for control of image acquisition are tabulated and explained. Long cable lengths can cause complications from skew and transmission line effects to digital control signals and noise pickup to analog signals. This design connected the control FPGA directly to the camera support printed circuit board which limited control signal traces to less than 6.5 cm. Similarly, the readout chip analog output signals had trace lengths of 2 cm to the analog-to-digital converter buffers. As desired, the noise of the external electronics was sufficiently low to allow evaluation of the noise of the CMOS readout. Thermal regulation of the detector was possible by construction of a vacuum tight clam-shell enclosure with a thermoelectric device and a water-chilled block. This enclosure was compatible with a pin-grid array detector carrier and a socket on

the support printed circuit board, which greatly simplified the implementation of the camera. Stud-bumping of high-resistivity detector layers to the CMOS readout allowed for photon detection. A simple process to modify a detector layer for efficient optical detection is described.

4.2 16×16 pixel CMOS readout

A 16×16 pixel chip was designed in TSMC 0.25 μm mixed-mode, metal-insulator-metal (MiM) capacitor, non-epitaxial process. The chip design was submitted to MOSIS for fabrication as part of a multi-project wafer run. The chip measured 4.01 mm × 4.13 mm and featured a 16×16 pixel array with 150 μm pitch, readout addressing registers, analog multiplexing of pixel output values, and four test pixels outside of the core array. A schematic of the high-level chip organization is shown in Figure 4.1. The purpose of this fabrication was to develop a chip that could be hybridized to silicon detectors already available in the laboratory so that photon detection could be confirmed and used for performance evaluation.

4.2.1 Pixel design

Tests of the first prototype CMOS chip determined that the pixel architecture with accumulation at the front-end was preferred. This pixel architecture with eight storage capacitors per pixel of size 300 fF and four front-end integration capacitors of sizes 700, 300, 500, and 466 fF was used throughout the entire array. Three modifications were made to the pixel design from the first submission. First, CMOS switches were added to the bottom-plate of the storage capacitors to decrease susceptibility to storage element cross-talk. Second, the output

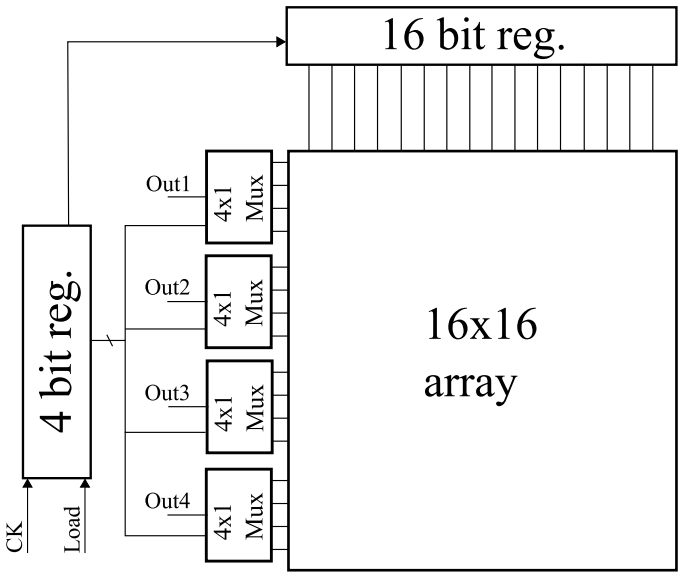


Figure 4.1: High-level organization of the 16×16 pixel CMOS chip submission. The 4 bit address shift-register controls four multiplexors that drive the four output signals to the ADCs and advances the slow 16 bit shift-register that selects the active column.

buffer was changed to a five-transistor NMOS input current-mirror differential amplifier due to the susceptibility to radiation damage of the folded-cascode output buffer found during tests of the first submission. Third, transistor sizing of the class AB amplifier was changed to increase the amplifier phase margin. The array was divided in half with the modified pixel in the eight columns first addressed by the slow 16 bit shift-register and the original pixel from the first submission in the second eight columns.[1]

4.2.2 ASIC power distribution

Three-side buttable PAD configurations constrain wire-bonds to only one edge of the readout ASIC, which forces careful consideration of the IR drop of supply voltages due to on-chip metal line resistance. The resistance of the pixel power

[1]Appendix computer file pointer for schematic: SchP2, appendix computer file pointer for layout: LP2, appendix computer file pointer for simulations: SimP2.

planes were manually extracted from the layout to calculate the IR drop at a given pixel along the column. The distribution of ground, V_{SSA}, is primarily in M5 and M1 at 3.6 □/pixel and 3.0 □/pixel, respectively (the process used has five metal layers; M1 is the metal layer closest to the substrate). Given a sheet resistance of 40 mΩ/□ for M5 and 80 mΩ/□ for M1 [122] the resistance of the ground distribution per pixel was found as $r_{pixVSSA} = 90\,\text{m}\Omega$. Similarly, the resistance per pixel of the power, V_{DDA}, distribution was extracted as $r_{pixVDDA} = 90\,\text{m}\Omega$.

The change of the voltage at the wire-bond to pixel p in a column is given by

$$\Delta V(p) = i_{pixel} r_{pixel} \sum_{n=1}^{n=p} (N - (n-1)) = i_{pixel} r_{pixel} (pN - p^2/2 + p/2), \qquad (4.1)$$

where i_{pixel} is the current drawn per pixel and is assumed constant along the column, r_{pixel} is the resistance per pixel, and N is the total number of pixels in the column. For the last pixel in a column the IR drop is $\Delta V(N) = i_{pixel} r_{pixel} (N^2 + N)/2$. The quadratic dependence of the voltage change at the last pixel upon the total number of pixels should be carefully considered when selecting the total size of a large area imager. The drop of the power supply, ΔV_{DDA}, and the rise of ground, ΔV_{SSA}, at the last pixel of a 100 pixel column is calculated as $(i_{pixel-\mu A})450\,\mu$V for each, where $i_{pixel-\mu A}$ is the static per pixel draw in microamps.

The effect of the power supply and ground drops on the current drawn by the front-end in-pixel amplifier have been calculated and verified in simulation. The results are shown in Table 4.1. The amplifier uses an NMOS current source so the current draw is most changed by a shift in the ground voltage, which modulates V_{GS} of the current source. Changes in V_{DDA} were confirmed in simulation to negligibly shift the current drawn by the amplifier. For small shifts in the source voltage of the transistor, the change in current can be calculated from the product of the transconductance of the current source with the shift in

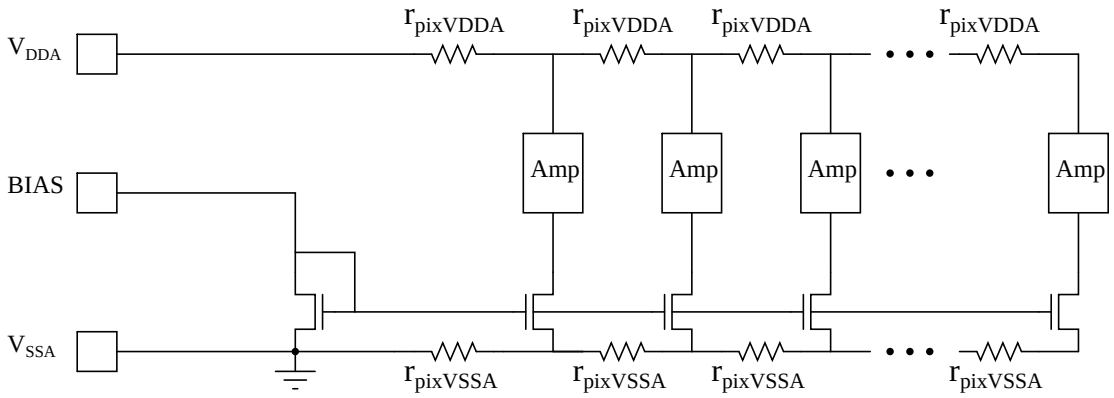


Figure 4.2: Schematic of a readout ASIC column to illustrate IR drop. Each pixel is represented by an amplifier (Amp) with its bias transistor explicitly drawn. The ground (V_{SSA}), power (V_{DDA}), and BIAS bonding pads are shown on the left.

ground voltage: $\Delta I_D = g_m \Delta V_{GS} = -g_m \Delta V_{SSA}$. For operation in strong-inversion the transistor transconductance is calculated as

$$g_m = \sqrt{2 I_D \beta_N} \tag{4.2}$$

where $(\beta_N)/(W/L) = 240\,\mu\text{A/V}^2$ [122]. The tabulated values anticipate a reduction in current drawn by the front-end amplifier at the end of a column of 15%, 17%, 20%, 24% for the four currents listed in Table 4.1 if the output buffer is assumed to draw $10\,\mu$A. The most critical design specification of this imager is the pixel speed. The estimations above suggest that IR drops should be manageable but are not far from being a problem. An array with more than 100 pixels per column or a more resistive distribution network than described could render parts of the ASIC too slow for single bunch imaging.

A maximum flux specification of 5×10^{11} x-rays/sec/mm^2 at 8 keV implies 76,500 x-rays/bunch/mm^2 for the bunch structure at the APS. If the input signal is assumed smoothed to 30 ns in duration by charge collection from the detector layer an instantaneous photo-current of $890\,\mu$A, results. This current draw is on the order of 10% of the current dissipated per column and should not markedly

Table 4.1: Calculated and simulated front-end amplifier current source transconductance to study effects from an increase in the ground potential in the pixel with respect to the ground potential at the biasing current mirror. I_D is the drain current through the current source transistor. g_m calc. is the transconductance calculated from equation 4.2. The next two columns were found by simulation of the amplifier current draw versus the increase of the in-pixel ground voltage. The simulated transconductance response of current drawn versus the increase in ground potential was extracted from the current drawn over a range of $\Delta V_{SSA} = 10\,\text{mV}$ and $\Delta V_{SSA} = 50\,\text{mV}$. The current drawn by the front-end amplifier is six times that drawn by the current source transistor.

I_D (μA)	g_m (μA/V) calc. square law	g_m (μA/V) sim. ($\Delta V_{SSA} = 10\,\text{mV}$)	g_m (μA/V) sim. ($\Delta V_{SSA} = 50\,\text{mV}$)
1.1	32.5	22	16.6
2.2	46	34.7	28.5
4.2	63.5	52.0	45.6
10.3	99.5	75.8	72.1

increase the IR drops.

The metal ground bus is also connected to the substrate throughout the pixel. These connections reduce the impedance of the ground distribution. The non-epitaxial substrate used has a bulk resistivity of $\sim 10\,\Omega \cdot \text{cm}$. If the substrate backside is metallized and grounded this connection would reduce the effect of IR drops. If ground IR drops are a particular concern an epitaxial process with a bulk resistivity of $\sim 0.01\,\Omega \cdot \text{cm}$ could be used to further increase the conduction through the substrate.[2]

In this layout local routing consumed M1 and M2, column-level routing of control signals was in M3, metal-insulator-metal capacitors consumed much of M4, which left M5 for distribution of the supplies. The extra metal layers offered by smaller feature size processes would significantly reduce the impedance of

[2] Another approach to IC power distribution connects the substrate to a separate node that is tied to analog ground off-chip. In this case no DC current flows through the substrate and the substrate conductance would not reduce ground IR drops. [109].

the power distribution since a single extra metal layer would double the number of layers available for power.

4.2.3 Readout addressing

The selection of a readout addressing architecture is a tradeoff between flexibility (random access) and off-chip simplicity (on-chip bit passing registers). Random access addressing requires a maximum of wire-bond pads and adds complexity to readout control signals. On the other hand, on-chip bit passing registers require fewer wire-bonds and limit the complexity of the readout control signals. For this submission a bit-passing register approach was chosen. A 4-bit shift register was used to control the 4 to 1 analog multiplexors (see Figure 4.1). The fourth element of the fast register advanced the slow 16-bit column register that selects the active column of pixels. For certain experiments a large chip design may benefit from the ability to readout only a portion of the array at a faster rate than the entire array (region-of-interest readout). In this case, random access addressing may be preferred. This design allowed the readout of a subset of columns but forced all rows to be read if the output from more than one column was desired.

4.3 Support electronics

An eight-layer support printed circuit board (PCB)[3] (shown in Figure 4.8 (e)) was designed that regulates supply voltages to the chip, has programmable potentiometers and buffering for chip biasing, holds four analog-to-digital con-

[3]Appendix computer file pointer for printed circuit board: PcbP2.

verters (ADCs)[4], and connects directly to the FPGA control board (see Section 4.4). The ADC chain noise was measured to be 240 μV with fixed voltages from the potentiometers connected to the inputs. The ADC voltage range is 2.5 V with a 153 μV least-significant bit step-size.

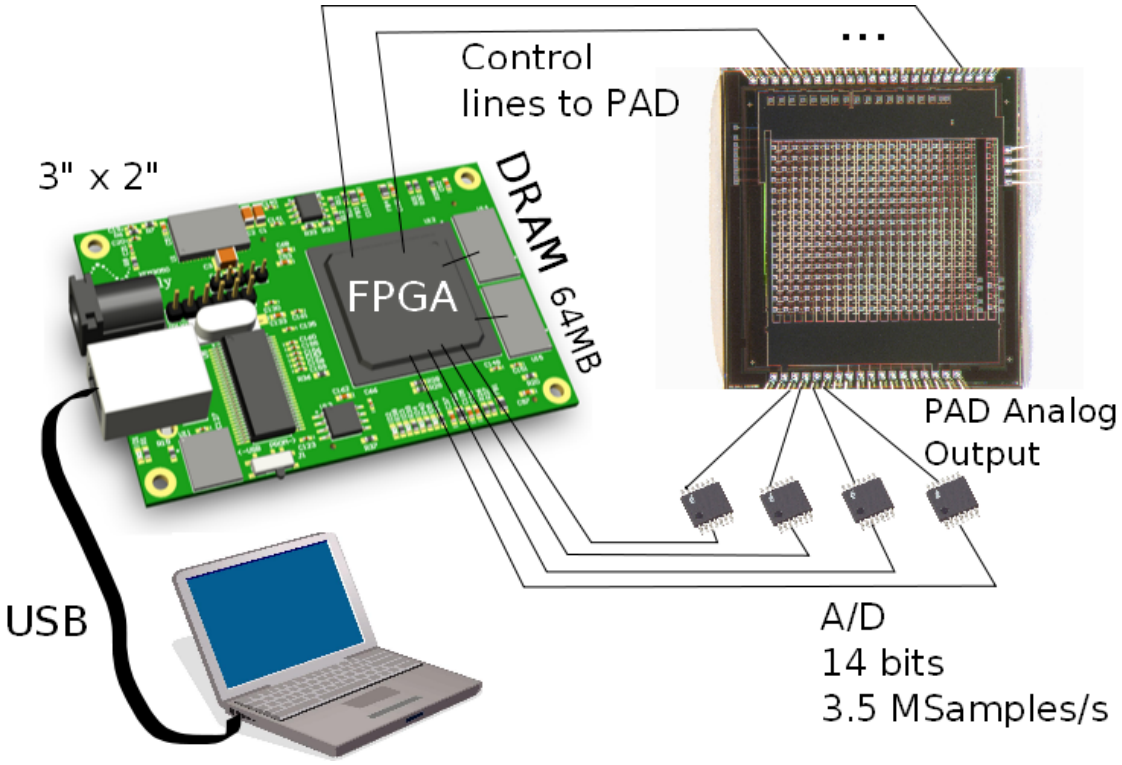


Figure 4.3: Schematic of the camera design that shows the propagation of data and control from the chip to a computer. The FPGA board drawing is from opalkelly.com.

4.4 FPGA and control software

A Field-Programmable Gate Array (FPGA) board (XEM3050 Opal Kelly, Portland, OR) with a Xilinx Spartan-3[5] FPGA was used to send digital control signals to the PAD, to temporarily store data from the analog-to-digital converters,

[4] ADC: Linear-Technologies 2355-14. Operational-amplifier buffer: Linear-Technologies 1801 (2 pF input capacitance)

[5] XC3S4000

and to transfer data to a computer. The FPGA board featured a USB 2.0 interface for download of the FPGA configuration and for communication between the FPGA and a PC. The board held two 32 MByte synchronous dynamic random access memory (SDRAM) chips which were used for data buffering and a programmable phase-locked-loop (PLL) that sourced the master clock of the FPGA.

Software control of the FPGA was written in Python.[6] The FPGA board vendor provides application programming interface code to implement three basic methods of communication through the USB interface between the FPGA and a computer. The three methods are wires which are simple asynchronous connections, triggers which are synchronous connections that signal an event, and pipes which are synchronous multiple byte transfers.[7] In this work, wire connections were used to address FPGA registers when a change of configuration was written, a trigger connection was used to signal the end of acquisition of a sequence of frames, and pipes were used to write data into FPGA registers and to transfer output data to the computer.

The code for the FPGA configuration was written in Verilog [123].[8] The ISE v9.1 software package from Xilinx (San Jose, CA) was used to create a programming file for the FPGA from the Verilog code. The FPGA configuration can be broken into a few distinct state machines with limited interaction as shown in Figure 4.4. The SPI controller programmed the digital potentiometers on the support board with the data loaded into the FPGA control registers by the control variable *pot_dict*. The integration state machine produced the control signals that were active during an exposure. At the end of an exposure the integration state machine triggered the readout state machine. This state machine sent signals to the PAD addressing registers and to the ADCs. During readout, data

[6] Appendix computer file pointer for FPGA control software: CSP2.
[7] http://www.opalkelly.com/library/FrontPanel-UM.pdf
[8] Appendix computer file pointer for FPGA code: FpgaP2.

from the ADCs was buffered into a 4-wide input 16-wide output first in first out (FIFO) buffer in the FPGA to meet the timing and data-width requirements of the SDRAM controller. The FPGA system was able to continuously read over 8,100 frames (each frame contained 4 kB of data and one 32 MB SDRAM chip was used for buffering) from the PAD before a USB transfer was required to a computer. Since another SDRAM chip is available on the FPGA board addition of a second SDRAM controller to the FPGA code would double the maximum number of frames per acquisition. A list of the control program variables that wrote data to registers in the FPGA are compiled and explained in Table 4.2.

FPGA code was often adapted from open-source projects available at OpenCores.org. Timing signals were created by modified versions of the 'Programmable Interval Timer' from OpenCores.org and the SPI controller was a modified version of the 'SPI controller core'. The WISHBONE interconnection architecture was adopted as a protocol for the addressing of the registers within the FPGA [124]. The SDRAM controller code was provided by the FPGA board manufacturer, Opal Kelly.

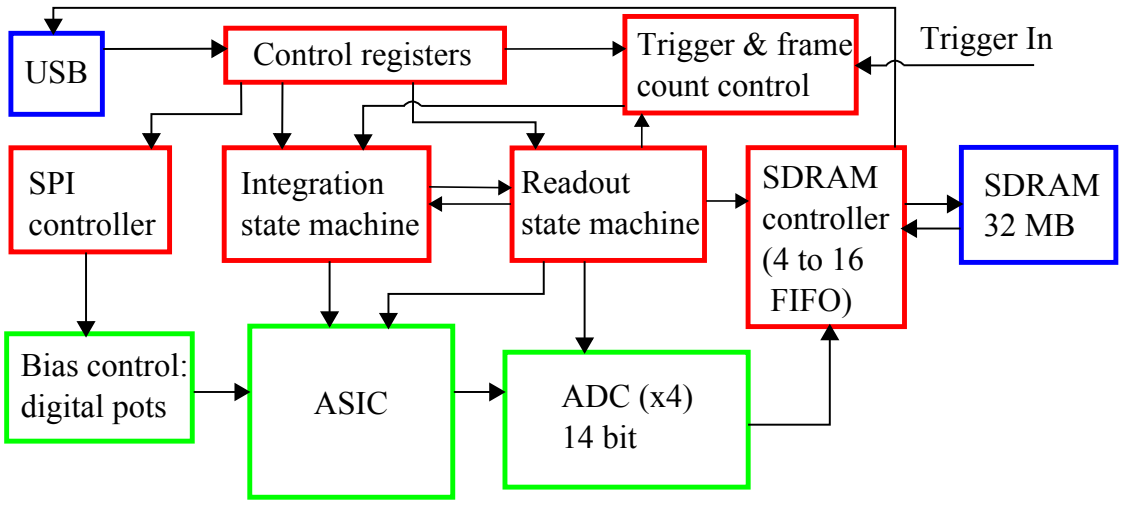


Figure 4.4: A block schematic that shows the organization and inter-block communication of the camera electronics. Items in red were part of the FPGA configuration, items in blue resided on the FPGA board, items in green were found on the support PCB.

4.4.1 Integration state machine

The integration state machine controlled signals that were active during an exposure. An example timing diagram is shown in Figure 4.5 for a capture that does not use the resampling functionality but, rather holds switches F1-F4 fixed (flash-capture). The exposure time of the first frame is given by t2-t1. At the end of the exposure the output is latched onto C_{S1}. The front-end is then reset and the process continues until values are stored onto all eight storage elements (the timing signals are shown for only four storage capacitors).

The exposure and reset times are set by the interval timer which produced intervals from 30 ns-21.4 s with a master FPGA clock of 10 ns. This range of 2^{31} was accomplished by a base 16-bit counter accompanied by a 16-bit modulo counter. For an interval of less than $\sim 655\,\mu$s the base counter covers the entire range and the modulo counter is not necessary. Greater intervals require the base counter to be driven by a version of the FPGA master clock divided down by the modulo counter.

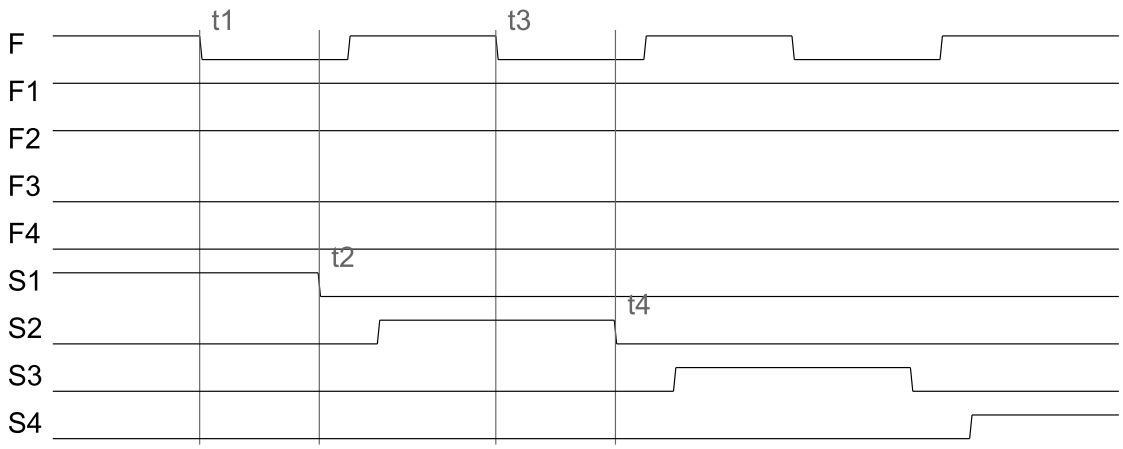


Figure 4.5: Digital control signals that are active during a flash-capture exposure. The switches are labeled as in Figure , with, for example, a switch driven by signal ϕ_F labeled simply as F. For this timing diagram a high signal indicates a closed switch and a low signal indicates an open switch, independent of transistor switch type. F is the pixel reset switch. When F is high signal current is drained to ground. F1-F4 are switches at the front-end integration capacitors. In this example, these signals are held constant and set the gain of the front-end to $1/(C_{F1} + C_{F2})$. S1-S4 are the switches that sample the front-end output onto the storage capacitors at exposure end. The exposure time of the first frame is set by t2-t1 (set by control software variable *int_time_us*). The time between the first and second frames is t3-t2 (set by control software variable *frame_time_us*). The exposure time of the second frame is set by t4-t3. Static operation of the front-end integration capacitors with C_{F1} and C_{F2} enabled and C_{F3} and C_{F4} disabled is set by control software variables *cap_reg* = [1,1,0,0] and *resample_bypass* = [1,1,0,0]. Flash-operation is ensured by control softwares variable *state_repeat* = 8. For simplicity only four storage element timing signals are shown, but the detector had eight.

Figure 4.6 shows an example timing diagram that implements resampling during an exposure. Between each accumulation all feedback capacitors are disabled and the front-end is reset. The number of storage capacitors (eight) does not match the number of accumulation elements (up to four). Because of this, each accumulation frame is sampled multiple times by the storage capacitors. The accumulation frames were sampled at the end of each of the last eight resamples. For example, if two accumulation frames are used, each accumulated

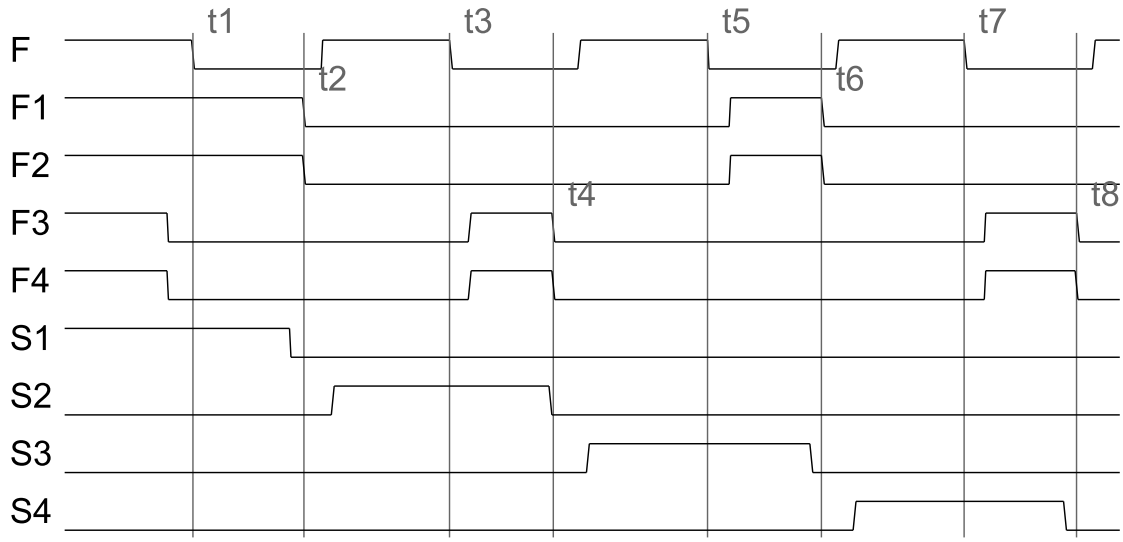


Figure 4.6: Digital control signals that are active during a resampling exposure with two separate resampled frames. In this example, the first resampling element is C_{F1}+C_{F2}. This element is accumulated onto twice during exposure times t2-t1 and t6-t5. The value of this element is stored by C_{S1} and C_{S3}. The other resampling element is C_{F3}+C_{F4}. This element is accumulated onto twice during exposure times t4-t3 and t8-t7 and is stored by C_{S2} and C_{S4}. This operation is set by control software variables *cap_reg* = [[1,1,0,0],[0,0,1,1]] and *resample_bypass* = [0,0,0,0]. *state_repeat* sets the total number of resampling operations. For this example, with two frame elements, the total number of accumulations on each element is *state_repeat*/2.

into N times, the first frame is sampled after accumulation $N-3$, $N-2$, $N-1$, N into storage elements C_{S1}, C_{S3}, C_{S5}, C_{S7} and the second frame is sampled in the same way onto the even numbered storage capacitors.

The integration state machine also controlled the charge injection circuit in each pixel. The pulse-width of the non-overlapping clocks that drive the injection circuit were set by the control software variable *chg_inj_us* and the number of injections per accumulation (or frame during flash-capture) is set by *chg_inj*. The exposure time must be sufficiently long to allow for the requested charge injection pulses to be sent. To store different voltages on the storage capacitors the FPGA code was designed to disable injection into frames specified by con-

trol software variable *inj_disable*. For example, with *inj_disable* = [1,0,0,0,1,0,0,0] charge is not injected into the pixel front-end during the frames sampled by C_{S1} and C_{S5}. This functionality allowed for testing of cross-talk between different storage elements.

4.4.1.1 Other possible imaging modalities

The ASIC switches can be driven in other ways. For example, the resampling control signals could be modified so that the front-end is not reset in between accumulations. In this approach the transition between accumulation frames would be dead-time free. Another possible imaging modality would be to operate two or four storage capacitors in parallel when resampling is used. If the speed requirements are not restrictive the increased load capacitance would decrease the noise sampled when the front-end output voltage is latched. Finally, FPGA code simplicity has generally insisted that the exposure time is equal for all frame elements. Experiments may benefit from independently programmable exposure and reset times for each frame element. The possibilities are vast with the primary limitation the time required to write the FPGA code.

4.4.2 Readout state machine

The signals of the readout state machine are detailed by an oscilloscope trace shown in Figure 4.7. The falling edge of PAD_CK advanced the 4-bit register and placed a new value onto each of the output lines (Out1-Out4 in Figure 4.1). The rising edge of CONV initiated ADC samples and the AD_CK signal updated the ADC output (the ADC output is not valid until the third rising edge after a CONV rising edge). The readout state machine FPGA code relied upon shift-registers that used parameters to set the number of clocks between sequential

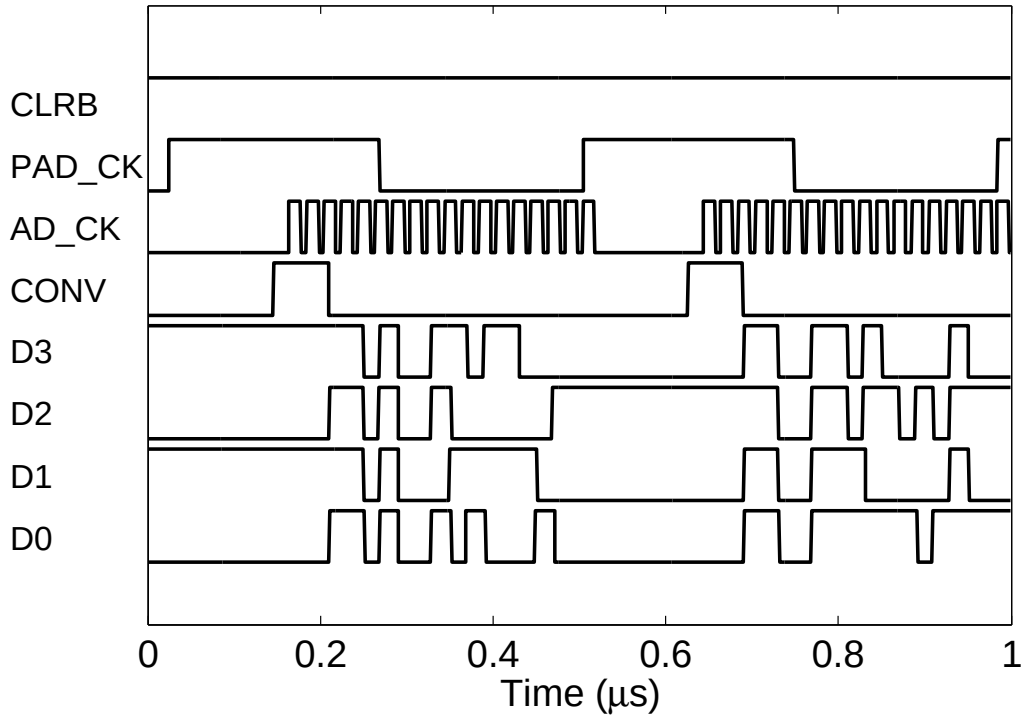


Figure 4.7: Digital scope-trace (high = 3.3 V, low = 0 V) that shows the control signals to the PAD and ADCs during readout. The output line of each ADC, D3-D0, is also shown.

events. Parameterization of the readout state machine was an effective tool to determine delay times for proper settling of the pixel output and the output signal from the analog multiplexor.

4.4.3 Control variables

Table 4.2: Description of the relevant configurable parameters within CamCtrl.py that were used to write to registers in the FPGA. Block indicates the logical section of the FPGA configuration in which the variable functioned (Int. - Integration state machine, Read - Readout state machine, Trig. - Trigger and frame count controller). Switch names are shown in Figure 4.5. Default FPGA configuration used a 10 ns period master clock which sets the minimum resolution of timing signals.

Variable	**Range and type**	**Description**	**Block**
chg_inj	0-255 (integer)	number of charge injections	Int.
chg_inj_us	μs	charge injection pulse width	Int.
inj_disable	length 8 bin.-array	1 disables charge injection for storage cap.	Int.
prst_ctrl	binary	0 sets front-end amplifier in unity-gain (Φ_F)	Int.
or_ctrl	binary	1 sets readout buffer in unity-gain (Φ_{OR})	Read
int_time_us	60 ns - 21.4 s	exposure time	Int.
frame_time_us	40 ns - 21.4 s	time between exposures	Int.
cap_reg	length 4×(1,2,or 4) bin. array	selects active integration capacitors	Int.
resample_bypass	length 4 bin. array	holds selected integration capacitors static (flash operation)	Int.
state_repeat	8 – 65535	number of cycles through cap_reg	Int.
repeat_cnt	1 – 255	number of resamples on each integration capacitor configuration	Int.
frame_num	1 – 8192	number of frames acquired before USB transfer of data to computer	Trig.
clk_per	μs (generally 60 ns or 120 ns)	period of AD_CK (determines readout rate)	Read
trigger_first	binary	if 1 trigger required for 1st frame of sequence	Trig.
trigger_others	binary	if 1 trigger required on frames other than 1st	Trig.
pot_dict	0-255 (8 element dictionary)	PCB potentiometer settings	SPI

4.5 Enclosure

The ASIC was packaged in a ceramic pin grid array (PGA) with 0.1″ pin pitch[9]. The PGA was mounted into a zero-insertion-force (ZIF) socket with a hole milled into the center that allowed a copper heat-sink to contact the back-side of the PGA. The support PCB and enclosure are shown in Figure 4.8.[10] The two aluminum pieces of the enclosure have an O-ring that contacts a metal ring on both sides of the PCB. A brass window with an epoxy attached 25 μm thick aluminized mylar x-ray transparent window (shown in Figure 4.8 (a)) covers the top-side aluminum piece of the enclosure. These pieces allow for evacuation of the environment of the detector to prevent water condensation when the detector is cooled. All electrical signals are transmitted into the enclosure through inner-layers of the PCB.

A cut through of the detector enclosure is shown in Figure 4.9. The cut-through is used to display aspects not easily depicted by a photograph. Labeled as 5 in Figure 4.9 is a thermally regulated copper cold-finger which the chip PGA rests on. A resistance temperature detector (RTD) with #8-32 threads purchased from Omega (Stanford CT, part #RTD-850) is mounted on the side of the cold-finger. Below the cold-finger is a thermoelectric cooling element (labeled 6) purchased through Digi-Key (CUI Inc., Tualatin, OR, part #CP60233). The cut-through shows the water channels in the back-side aluminum enclosure (labeled 7). With a water-temperature of 9 °C the thermo-electric cooling was able to reach a cold-finger temperature of -24 °C with the ASIC biased. All pieces of the enclosure were expertly machined by Martin Novak.

[9] MOSIS package name PGA108M

[10] Appendix computer file pointer for enclosure design: EncP2

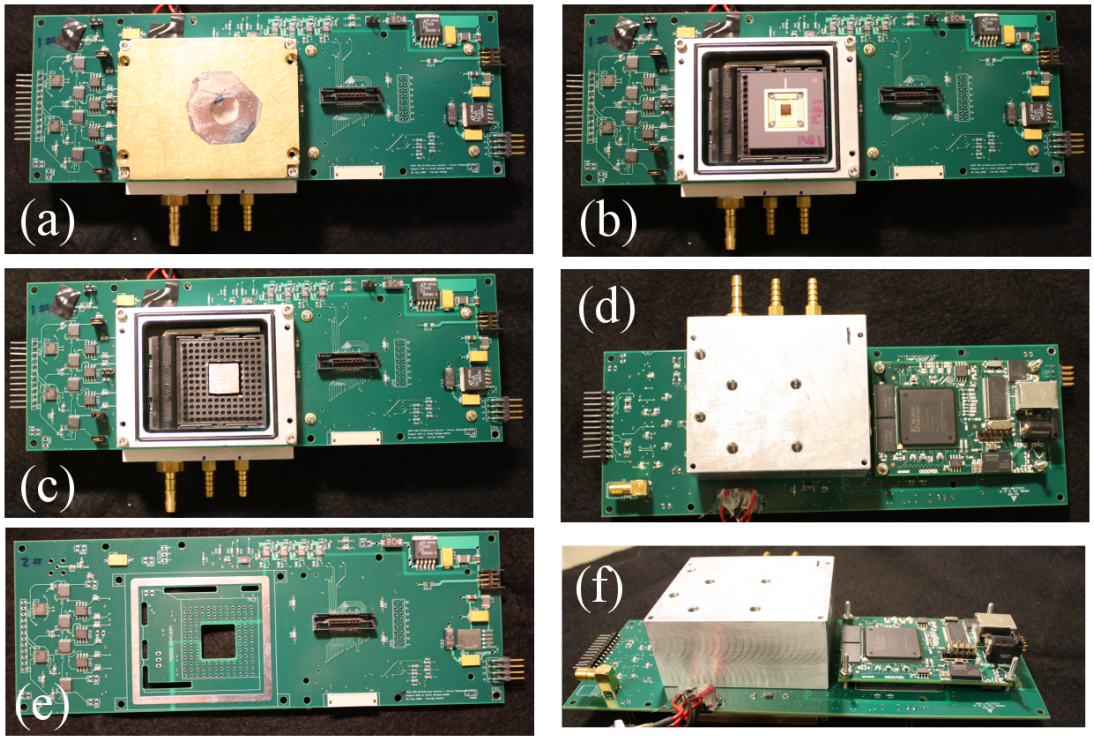


Figure 4.8: Photographs of the support PCB and enclosure from different angles and at different levels of construction. (a) The system entirely assembled from the top-side. An x-ray transparent aluminized mylar window covers a hole in the top brass cover. Three barbed hose-fittings are shown at the bottom of the photograph. The larger left-most hose-fitting is a vacuum port. The other two are connections for cooling water. (b) The enclosure with the brass cover removed to reveal the PGA and chip mounted in the ZIF socket. (c) The chip is removed to show the copper cold-finger that protrudes through the ZIF socket and contacts the PGA bottom-side. (d) PCB photographed from the back-side so that the control FPGA board on the right and the back-side aluminum water-chilled block with mounting holes are shown. (e) PCB without the enclosure or ZIF socket to show the hole for the copper-cold finger and the metal ring for O-ring contact. (f) The back-side is shown from the side. The water-chilled aluminum block is $1\frac{1}{4}''$ thick. The support PCB measures $8.0'' \times 2.85''$.

4.6 Hybridization

To test photon detection readout ASICs were hybridized to high-resistivity silicon detector layers. The detector layers were 16×16 pixel detectors n-type

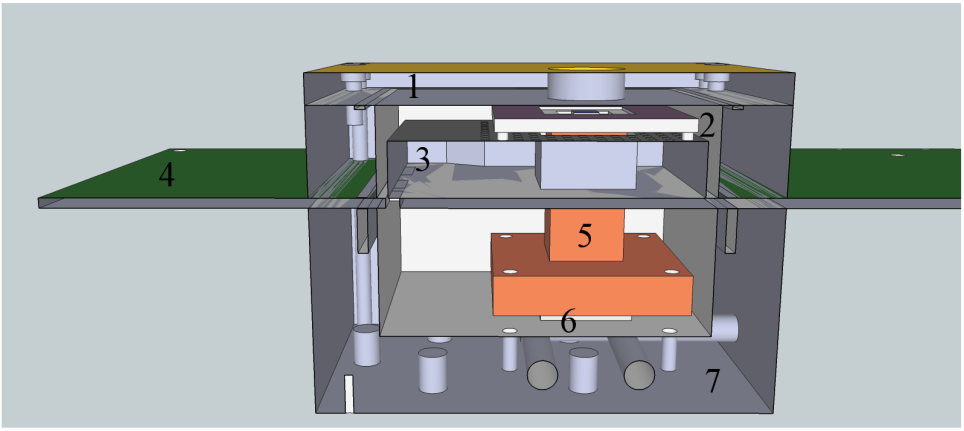


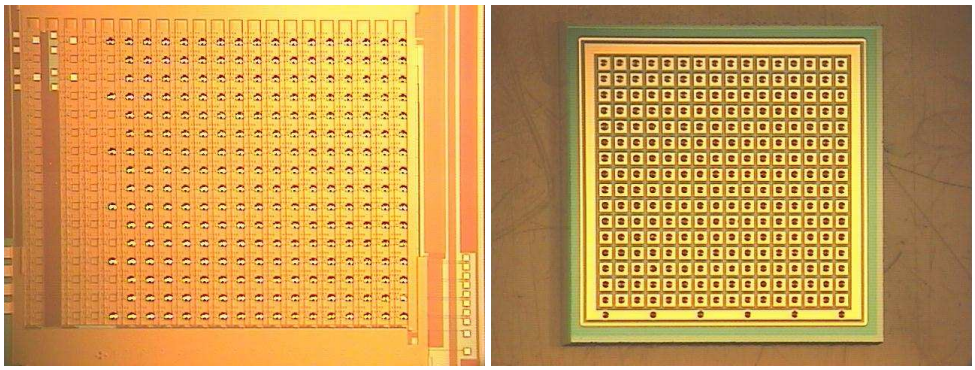
Figure 4.9: Cut-through of the three-dimensional drawing of the detector enclosure. The labeled elements are: 1) top brass cover with circular window, 2) chip and PGA, 3) ZIF socket with a hole milled into the middle, 4) support PCB, 5) copper cold-finger, 6) thermo-electric cooling element, 7) aluminum water-cooled back-side enclosure piece. Drawn with Google sketchup.

500 μm thick layers fabricated by SINTEF (Oslo, Norway) with a gold pad metallization (these chips were designed for MMPAD developments and were supplied by Tom Hontz from Area Detector Systems Corporation). p+ pixel implants are formed on the bump-bonded side and an aluminized n+ ohmic contact is applied on the x-ray incident side for the application of a bias to deplete the thickness of the sensor.

To bump-bond the detector layers to ASICs the first consideration was that multi-project wafer runs from MOSIS return diced chips. Because of this bump-bonding at the wafer level was not possible. Gold stud bump bonding using conductive adhesives is a flip-chip process compliant with small diced chips and was determined to be appropriate for this work [125].[11] This process attached gold stud bumps to the aluminum pad on the CMOS chip by intention-

[11]Polymer Assembly Technologies (Research Triangle Park, NC) contact: James Clayton

ally removing the wire from a thermosonic wirebond to leave only the ball-bond (Figure 4.10(a)). Also, a conductive polymer epoxy bump (volume resistivity of 0.0005 Ω-cm) is placed on the pads of the detector through a stencil screen (Figure 4.10(b)). The gold ball and detector pad are either in contact or extremely close such that the contact resistance was anticipated to be negligible (no issues that could be attributable to contact resistance were found when testing high-speed response) [126]. Of fourteen ASIC chips provided to Polymer Assembly Technologies only seven were successfully stud-bumped. The cause of the gold wire-bonding problem was unknown but hypothesized to be due to surface contamination.



(a) (b)

Figure 4.10: Photos of (a) the read-out ASIC with stud-bumps attached and the detector chip with epoxy applied (courtesy of James Clayton from Polymer Assembly Technologies).

4.6.1 Detector aluminum etch for laser experiments

An intense synchrotron x-ray beam may have a flux of 1×10^{13} photons/s which corresponds to a power of 13 mW at 8 keV. A similar output power of 5 mW can be had from a simple hand-held laser pointer. The ability to test with vis-

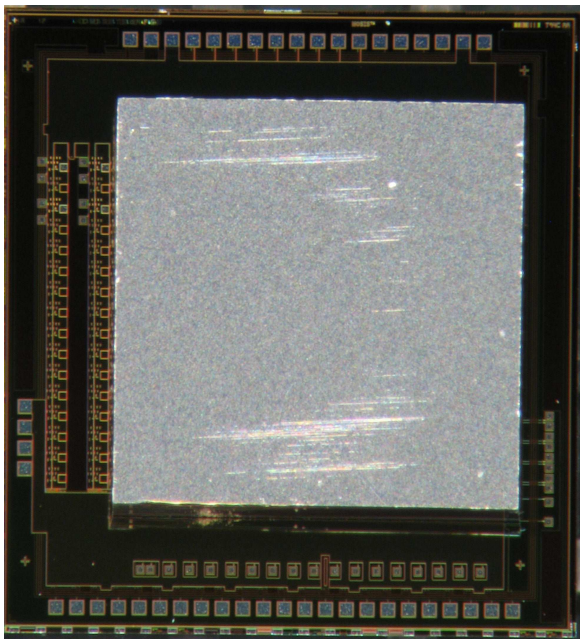


Figure 4.11: A microphotograph of a detector layer hybridized to a CMOS readout. The chip shown in Figure 4.10(b) was flipped onto the chip of Figure 4.10(a) to form the hybrid shown.

ible laser light was highly desired due to the ease of use of a standard laboratory laser and the possibility of intensity modulation with a function generator. However, the detector top-level aluminum metallization was found to transmit only 1.6×10^{-5} of the incident light at a wavelength of 635 nm.

To remove the aluminum top-layer from a detector chip a 2 μL drop of 85% phosphoric acid was placed onto the detector with a pipette while working under a microscope. As shown in Figure 4.12, after a two hour etch a central circular region of ≈ 2 mm in diameter was free of aluminum. Then the phosphoric acid was removed with a deionized water rinse and the chip was dried in a vacuum oven. After removal of the aluminum a photocurrent of 170 μA was measured with a 0.5 mW laser incident on the bare silicon (detection efficiency of 67%).

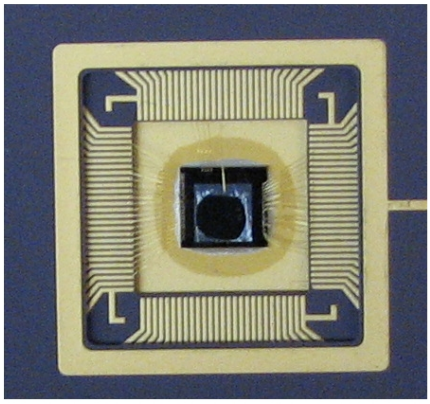


Figure 4.12: A photograph of a hybridized detector in a PGA with the top-layer aluminum removed for enhanced visible detection. The aluminum is removed in the center of the detector layer while the outer perimeter is left so that the wire-bond remains.

4.7 Conclusions

The readout control system developed allowed for flexible control of the ASIC to facilitate understanding of its performance. By far this was the most reliable system, in terms of computer hangs and required reboots, that I used throughout my work with various PAD control systems. This was not an accident but, rather, was because the computer operating system was not required for any timing critical operations. Further, the code for communication between the FPGA and computer was provided and validated by a commercial vendor. During a sequence of exposures FPGA state-machines were entirely in control. The operating system software waited for a signal that indicated the end of the exposure sequence from the FPGA. Once the end signal was received data was transferred from the FPGA board SDRAM to the control computer at a rate reported by the FPGA board vender of ~35 MB/s.

Temporary data-buffering without continuous stream to hard-disk may only seem feasible because of the small pixel-count of this detector. Consider a larger

area PAD of 400×200 pixels with eight storage capacitors per pixel and two bytes per analog-to-digital conversion. This detector would produce 1.28 MB per image, which, if readout in 10 ms, would produce a continuous data-rate not above 128 MB/s). A 4 GB DDR module for an FPGA board could hold over 3,000 images before a write to hard-disk is required. If even more buffering capacity is required some FPGA boards offer SATA connectors that could be connected directly to a fast, possibly solid-state, hard-disk. Solid-state disks are available that have a SATA interface and 160 MB/s write speeds. Nuvation offers an Intellectual Property core for Altera FPGAs for configuration as a SATA host controller. With this configuration data acquisition would utilize only FPGA state-machines and would not require any interaction with a control computer until acquisition was complete. Transfer of data to a control control could occur over USB-2.0 or gigabit ethernet following the completion of an acquisition. As an experimenter I would rather sacrifice slightly on continuous data-rate and avoid time-consuming and frustrating system restarts.

CHAPTER 5

EXPERIMENTAL EVALUATION OF 16×16 PIXEL CAMERA

This chapter presents experimental evaluation of the 16×16 pixel x-ray camera described in the previous chapter. Fundamental tests without photo-signal input are presented that evaluate the detector noise, and linearity, and also the parameters of the accumulation functionality. High-speed response was tested with both the in-pixel charge injector and pulsed laser sources. These tests not only probe the functionality of the readout ASIC but investigate the implementation of the FPGA based control and readout. The accumulation functionality was studied and used to extract the power spectral density of the intensity of an input optical signal. A bare readout chip was dosed up to 600 kGy(Si) and the pixel performance was evaluated at multiple levels of accumulated dose. Functionality remained for the pixel modified for improved hardness after an accumulated dose of 600 kGy(Si) at the CMOS electronics.

The high-flux x-ray response of the camera was tested at CHESS G3 hutch. The detector was shown to resolve individual bunch trains from the synchrotron at levels of up to 3.7×10^3 x-rays/pixel/train. The x-ray camera proved to be a unique device for the purpose of characterization of the intensity and position fluctuations of the incident x-ray beam at high-speeds. Single bunch-train intensity measurements were made to a repeatability of 0.4%–almost entirely limited by Poisson statistics. Fast horizontal position fluctuations were detected and attributed to known betatron oscillations of the positron cloud within the synchrotron ring.

5.1 Noise performance

Pixel operating parameters *prst_ctrl* and *or_ctrl* (see Table 4.2) were used to study the noise performance of the pixel. The measurements, described below, are shown in Table 5.1 and illustrated in Figure 5.1. The noise of the readout chain and ADC system was evaluated with Φ_{OR} closed which placed the pixel output buffer into unity-gain. This configuration measured the noise of the pixel output buffer, row output buffer, off-chip ADC buffer, and the ADC, while it eliminated any contribution from the front-end amplifier. Standard Φ_{OR} operation was combined with continuous reset of the pixel front-end (Φ_F closed) to evaluate the noise contribution from sampling the front-end amplifier output onto an analog memory capacitor (C_S) and configuration of the in-pixel output buffer with capacitive feedback to drive the value stored on C_S. The noise of standard pixel operation was measured by opening Φ_F, which adds reset noise at the pixel input and the increase of the noise transfer of the front-end amplifier to the other noises measured in the first two tests. For these measurements the feedback capacitance was 1966 fF. The dependance of front-end reset noise upon integration capacitance will be made clearer by studies of noise growth versus the number of accumulations. Also shown in Table 5.1 are the estimated isolated contributions from each sampling operation. For this calculation the isolated noise sources were assumed to add in quadrature and a measurement of 240 μV for the noise of the off-chip ADC buffer and ADC was used.

The noise measurements confirmed that the high-speed ADC system with short connections from chip output to converter input held the noise of the readout chain below the noise of the pixel. The smaller noise contribution imparted by the external electronics revealed that the read-noise measured with the first prototype ASIC (730-750 μV) was not limited by the pixel. These mea-

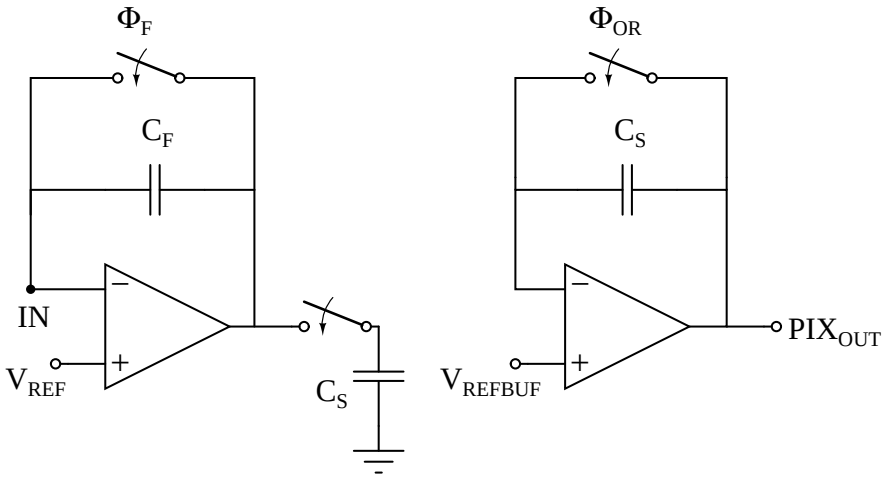


Figure 5.1: A simplified schematic to illustrate the noise tests. On the left the front-end amplifier is shown. On the right the in-pixel output buffer is configured in capacitive feedback. Switches not shown allow the transition from the configuration shown on the left for image acquisition to the configuration on the right for storage element readout.

Table 5.1: RMS noise measured for three operation modes in units of μV. Measurements for the two array halves are written as original pixel design; modified pixel design. The isolated contributions are calculated from the measured values. $ISO_1^2 = M_1^2 - M_2^2$, $ISO_2^2 = M_1^2 - M_3^2$, and $ISO_3^2 = M_3^2 - (240\,\mu\text{V})^2$.

Chip	**Standard operation (M_1)**	**Φ_F closed (M_2)**	**Φ_{OR} closed (M_3)**
Bare ASIC	554; 445	548; 434	334; 316
Hybrid	559; 445	559; 435	335; 317
Isolated contributions			
Chip	**FE reset (ISO_1)**	**FE sample & OutBuf (ISO_2)**	**ASIC readout chain (ISO_3)**
Bare ASIC	81; 98	434; 297	232; 206
Hybrid	0; 94	447; 298	234; 207

surements compare favorably to the RMS read-noise of 1.5 mV of the first MM-PAD camera [50]. The noise in standard operation of the small area camera also approached the low-gain noise of the LCLS detector, 280 μV, and improved upon the high-gain noise of the LCLS detector, 750 μV [51]. Of course, compared to the other designs referenced above the 16×16 pixel camera has the lowest con-

version gain for increased saturation value. The RMS equivalent noise charge (ENC) of the modified half of a hybridized PAD for flash-mode operation were 1000, 1445, 2800, 3415, and 5500 e^- for capacitive feedback configurations of 300, 466, 966, 1200, and 1966 fF, respectively (the noise of the other half, due to differences in the sampling stage, was around 20% greater). Therefore, a signal-to-noise of 2.2 for the detection of a single 8 keV x-ray is possible at the highest front-end gain setting.

5.2 Linearity and voltage range

The linearity of the PAD response was studied with the in-pixel charge injector. Figure 5.2 shows the average pixel output plotted versus the number of charge injection operations and the deviation from linearity as percent of the pixel full-well plotted versus the output voltage. The results of Figure 5.2 are differentiated by modified pixel design (top) and original pixel design (bottom). The voltage swing with less than 1% non-linearity was 2.06 V for the original pixel design and 1.88 V for the modified half. The lower range of the original pixel extends further toward ground than the modified pixel by around 200 mV. The differential folded cascode in-pixel output buffer in the original pixel design used a low dropout current mirror which allowed for a large voltage swing. However, this amplifier architecture proved to be insufficiently radiation robust (see Sections 3.5.2.6 and 5.6). The redesign of the pixel output buffer for improved radiation robustness sacrificed voltage swing. These linearity measurements are representative of the readout chip but are not definitive since adjustments of reference voltages and amplifier bias levels will induce changes in the linear voltage range. Voltage swing improvements could be made through adjustments of the reference voltages V_{REF}, V_{REFBUF}, and the reference voltage to

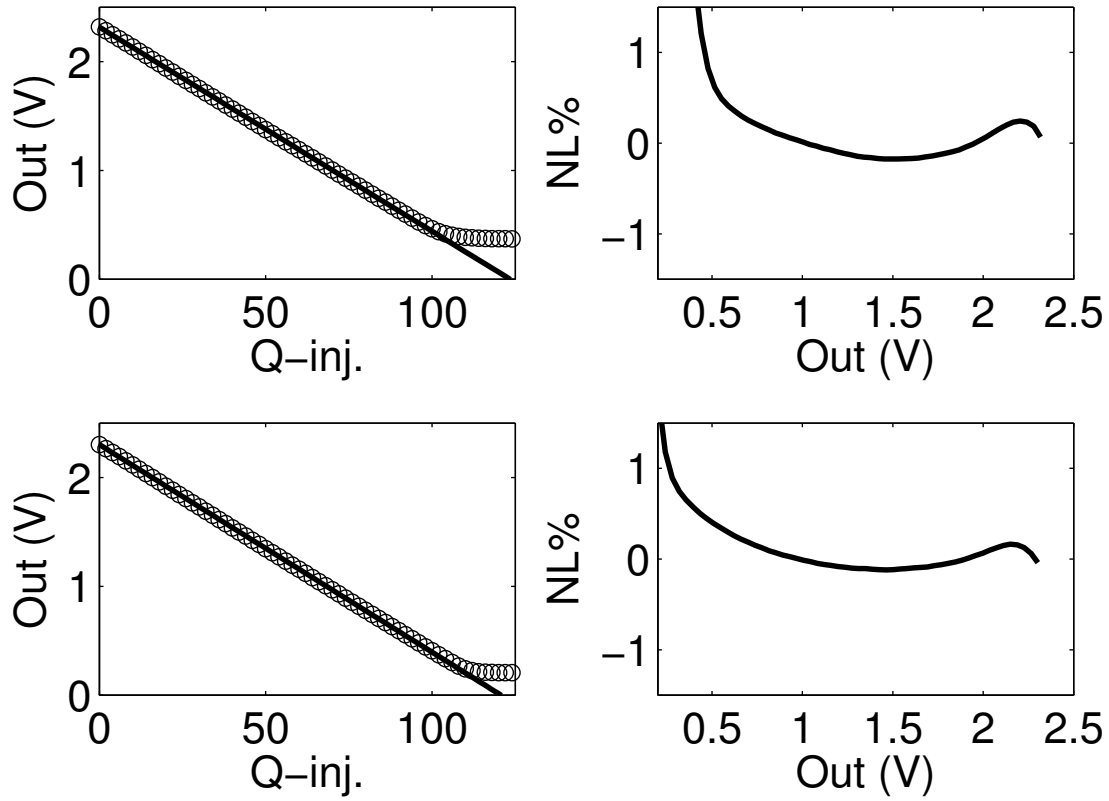


Figure 5.2: Detector linearity studied with the in-pixel charge injector. On the left the pixel output (∘) and a linear fit (solid line) is plotted versus the number of charge injections (Q-inj.). The right shows the deviation of the measured values from the linear fit as a percent of the full-well value. The top panels show the measurements from the modified half of the pixel array. The bottom panels show the results from the original half. These experiments used a bare ASIC with the front-end gain configured as $C_F = 300\,\text{fF}$. Each charge injection operation corresponds to roughly 5.75 fC. For this measurement V_REF = 170 = 2.20 V, V_REFBUF = 80 = 1.04 V, VREF_BP = 70 = 0.91 V (see Appendix for detailed explanation of potentiometer settings).

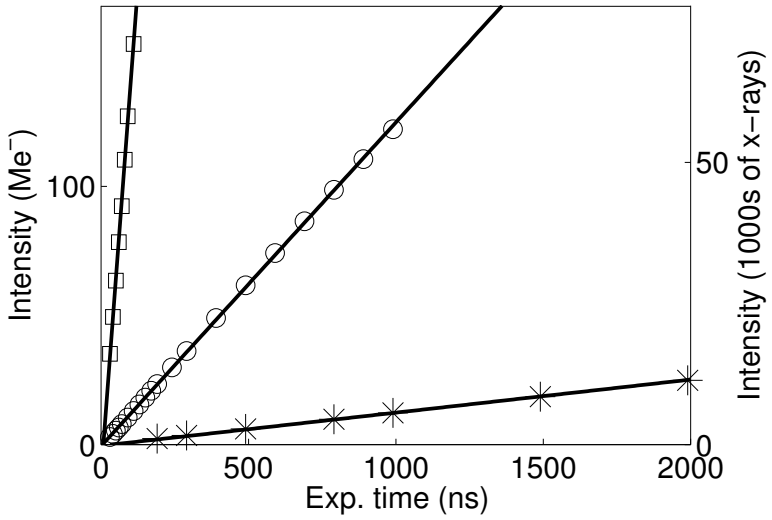
the bottom plate of the analog storage capacitors.

The PAD linearity was studied at high input photocurrents using the hybridized device with the top layer aluminum removed (see Section 4.6.1) illuminated by a laser. A helium-neon laser was used with a wavelength at 633 nm and a 0.5 mW maximum output power (Melles Griot, Albuquerque, NM, Model 25-LHP-213-249). To vary the incident intensity the laser was attenuated with

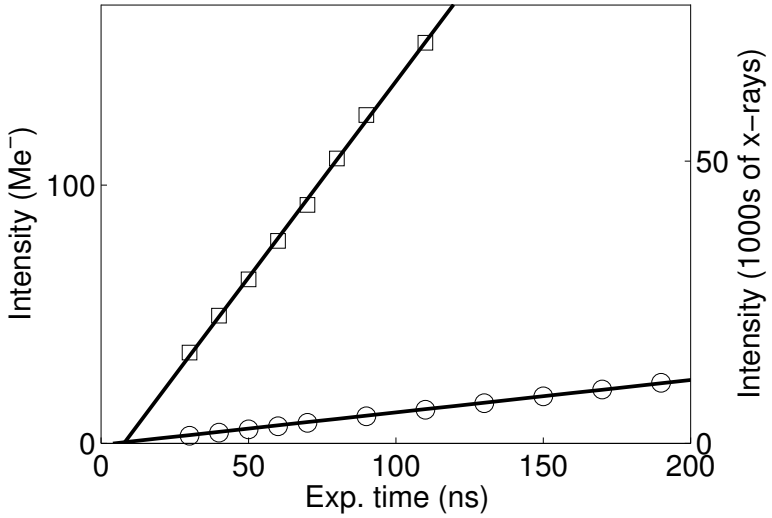
neutral density (ND) filters. Figure 5.3 shows the integrated intensity (in millions of electrons on the left and equivalent 1000s of 8 keV x-rays on the right) in the laser spot versus the exposure time acquired with three levels of attenuation. Figure 5.3(a) displays the output for exposure times up to 2000 ns and (b) shows the same measurements focused on the range of exposure times up to 200 ns. Figure 5.3 confirms the resolution of 10 ns of the FPGA timing circuits. The successful development of the FPGA control is as crucial as the ASIC design for these measurements.

The total photocurrents measured were 243 μA, 20 μA, 2.1 μA, for no filter and filters with optical densities of 1 and 2. The maximum per pixel photocurrent was 12 μA without attenuation, which is comparable to the static bias current of the front-end amplifier and the response remains linear. The intercepts of Figure 5.3(b) were near to zero, the deviation may be because the effective exposure time was slightly different than what was programmed into the FPGA. This could be caused by different delays for rising and falling edges of digital buffers.

The photocurrent produced by the unattenuated laser is equivalent to the signal from an 8 keV x-ray flux of 7×10^{11} x-rays/s. Such a flux is around a factor of 1000 greater than what is accessible with laboratory x-ray sources. Similar fluxes are accessible at the synchrotron but debugging at high-fluxes in the laboratory before synchrotron tests was very valuable. A detector without an aluminum top-layer and a low to moderate output power laser source allowed for testing of the PAD in the laboratory at photocurrents similar to the most intense synchrotron beam-lines.



(a)



(b)

Figure 5.3: Detector linearity at nanosecond exposure times tested with a laser source. □ used the laser unattenuated, ○ and ∗ used neutral-density filters of optical densities of 1.0 and 2.0, respectively (×10 and ×100 attenuation). Solid lines are a linear fit to the measured points.

5.3 High-speed performance

A laser diode with analog modulation at up to 20 MHz with a wavelength of 635 nm and maximum output power of 3 mW (Newport Corp., Irvine, CA, Model LQA635-03C) was used to test high-speed collection of a pulsed input.

The laser modulation input was driven by a function generator from 200 mV (off) to 1 V (on).[1] The modulation input was driven high for a duration of 40 ns to produce a short burst. A delay generator (Stanford Research Systems, Sunnyvale, CA, Model DSG 535) drove the PAD trigger input to control the delay between laser pulse and PAD acquisition and was configured such that the laser pulse was coincident with the acquisition of the fourth in-pixel storage element. The PAD exposure time was set at 90 ns.

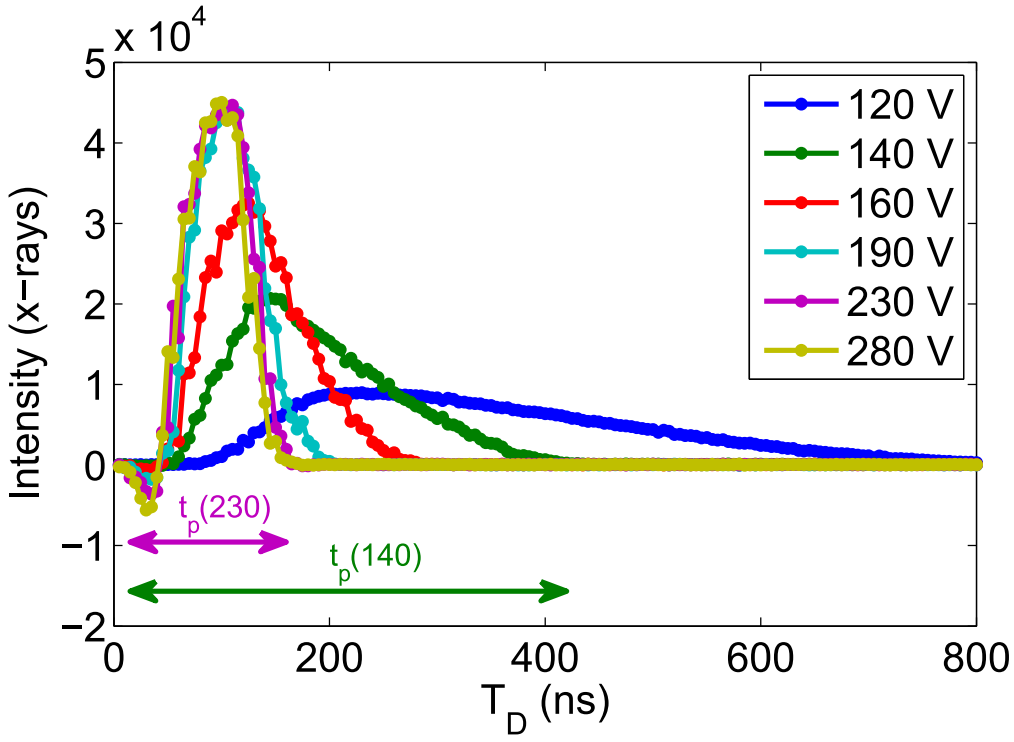


Figure 5.4: Integrated intensity in a detected laser spot (in equivalent 8 keV x-rays) for a pulse of 40 ns duration versus the delay between PAD acquisition and the pulse. The experiment was repeated at multiple values of the detector layer bias (V_{bias}), which are indicated in the legend. Data was acquired with a 90 ns exposure time, C_F = 1000 fF, and with a front-end amplifier dissipation of 8.1 μA. t_p indicates the measure of the collection time duration discussed in the text for bias levels of 140 and 230 V.

[1]It was found that the speed and intensity of the laser pulse depended on the modulation voltage for the off-state; a brighter pulse is produced during the duration of the high control voltage when the low control voltage is near to the lasing threshold.

Figure 5.4 shows the integrated intensity in the detected laser spot versus the delay between the laser pulse and the PAD exposure window (T_D) acquired at multiple values of the detector layer bias. At larger T_D the PAD was started later with respect to the laser.[2] The interval from when the laser pulse arrived (as measured by the experiment at a reverse bias of 280 V) to when the integrated signal fell to 1% of the maximum signal is indicated as t_p for bias levels of 140 and 230 V in Figure 5.4. Table 5.2 lists the measured collection time and the collection time reduced by the exposure time of 90 ns for all bias levels. These results show that the response time was slowed minimally by the pixel electronics.

Table 5.2: Laser pulse collection time for different detector bias levels. The third column indicates the measured collection time minus the exposure time of 90 ns. This measure should be the sum of the laser pulse-width, charge collection time, and response time of the pixel electronics.

V_{bias} (V)	t_p (ns)	t_p-90 ns
120	1005	900
140	405	315
160	265	175
190	185	95
230	145	55
280	145	55

Figure 5.4 and Table 5.2 emphasize the importance of detector overdepletion for prompt charge collection. For example, at a detector bias of 190 V, which should fully deplete the detector, the charge collection time is expanded by 40 ns from the collection time measured at a detector bias of 230 V. From these measurements a detector bulk resistivity of 6 kΩ·cm was estimated.

The absorption length of silicon at 635 nm is 2.5 μm [127] which implies that

[2]During post-processing, the output from in-pixel analog storage elements 4 through 8 was merged since the delay between PAD acquisition and laser pulse was only varied by 225 ns, which was not sufficient to follow the entirety of the signal collection with a single in-pixel storage element at low detector layer biases.

0.45 of the incident photons are absorbed in the first 1.5 μm of the detector layer, which is a heavily-doped, field-free ohmic contact. A fraction of the holes produced in this region will diffuse out of the ohmic contact and then drift through the detector bulk to the pixel electrodes. The carrier lifetime within the ohmic contact, and subsequently the fraction of carriers that escape, depends on the doping and surface passivation [128]. Holes diffuse a distance of 1.5 μm in an average time of 1 ns in silicon at room temperature, which proves that collection times measured with laser illumination will not be noticeably increased due to a slow component of the signal current from carriers that are created in the heavily doped ohmic contact.

5.4 Storage element leakage

The analog storage element leakage currents were studied by varying the hold-times of the storage elements. The in-pixel charge injector allowed measurement of the leakage at all levels of voltage held. Figure 5.5 shows the results at three separate temperatures. At temperatures of 18, 1, and -24 °C the measured leakage (at the output voltage that produced the largest leakage) was 2.1, 1.0 and 0.4 fA. Equation 3.23 predicts a stronger dependence on temperature; the discrepancy may arise because transistor switch subthreshold conduction is not entirely the source of the leakage. The voltage signal stored at the analog memory from an 8 keV x-ray is 180 μV with the largest feedback capacitor configuration. At a temperature of -24 °C a hold time of less than 13.5 ms is required to maintain the storage leakage under the equivalent of one-tenth of an 8 keV x-ray.

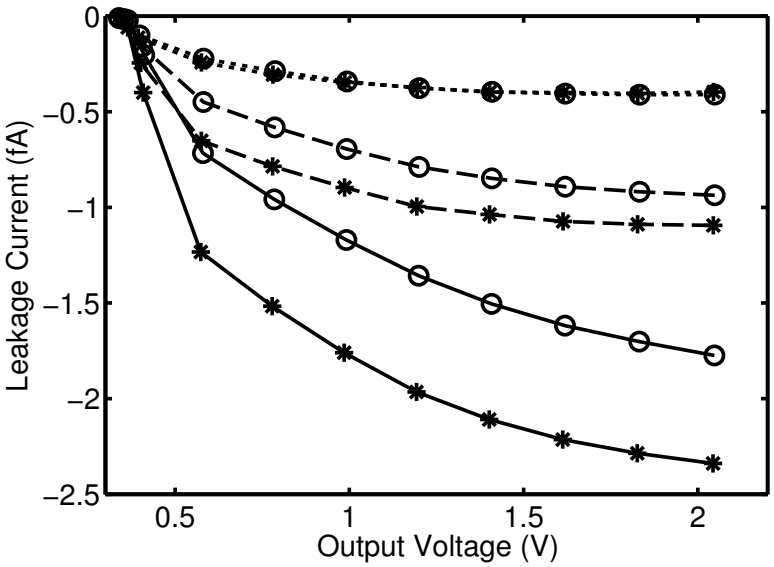


Figure 5.5: Leakage current from analog storage elements C_{S1} ($\circ$) and C_{S5} ($*$) (see Figure 2.4 or Figure 4.5) at three temperatures versus the voltage output from the pixel. Lines delineate temperature of measurement: solid-line T = 18 °C, coarse dashed-line T = 1 °C, and fine dashed-line T = -24 °C. A negative leakage current indicates that the pixel output voltage decreased as the hold-time increased. Data shown is from the modified half of the ASIC (as discussed in section 4.2.1).

5.5 Accumulation

Ideally, the accumulation operations are noise-less and inject no charge into stored signal. Unfortunately, this is not possible. In this section the charge signal and noise imparted per accumulation is presented. The charge injected per accumulation was characterized versus the front-end feedback capacitor engaged and was found to be around or less than 1% of the full-well. Since the charge injected per accumulation was found to depend upon the signal integrated a technique to correct for this source of non-linearity is discussed. The noise charge imparted per reset operation was measured for both hybridized and non-hybridized devices and found to follow the form of $\sqrt{kTC}$, where C is the capacitance at the pixel-front end. The noise per accumulation is such that

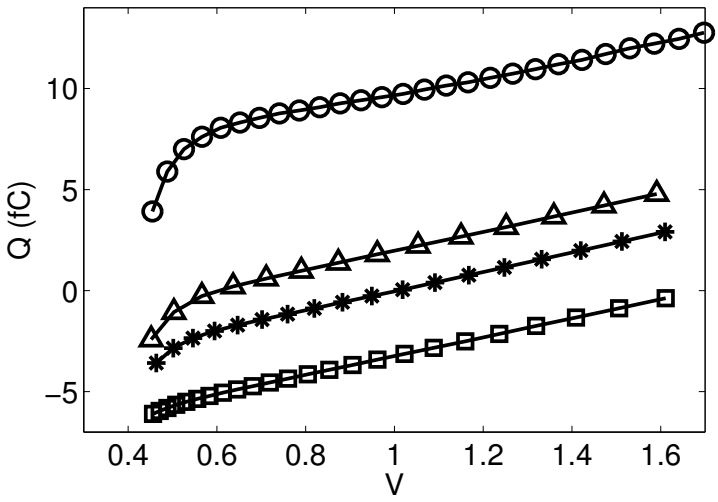
around 25 accumulations were possible before the noise induced approaches the fixed detector read-noise, which displays the utility of the accumulation functionality to lift low signal levels above the detector read-noise. Two demonstration experiments are presented to show the unique possibilities that this functionality facilitates.

5.5.1 Charge injected

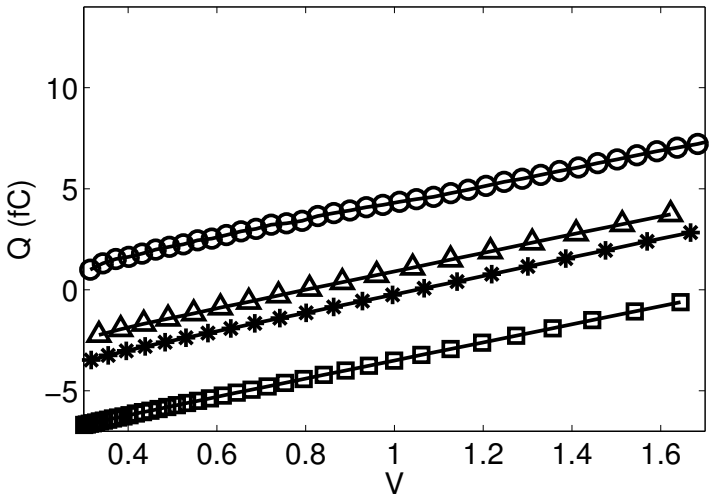
The charge injected per accumulation operation was measured for a hybridized device at $T = 18\,^{\circ}\mathrm{C}$ in an experiment that accumulated up to 446 times on each accumulation element under test. Since the charge injected per accumulation was found to be zero at a particular voltage for some values of the feedback capacitance, the in-pixel charge injector was used to inject charge once per accumulation to ensure that the pixel value did not stall. In a separate experiment the signal per charge injection operation was measured without accumulations so that it could be subtracted from the accumulation data. The charge injected per accumulation operation is plotted versus the pixel signal voltage in Figure 5.6.

Earlier Cornell prototypes have measured 7 fC injected from the opening of switch Φ_F [95] (see Figure 5.7). Since each accumulation operation requires three separate switch operations the results of Figure 5.6 (less than 7×3 fC) suggest that the dummy switches (section 3.2.3.1) may have reduced the charge injected per operation. The largest magnitude of charge injected for the 466 fF and 500 fF feedback capacitors was 4 fC, which means that the charge injected per accumulation encompasses 0.6% of the full-well. The maximum percent of the full-well per accumulation with the 300 fF feedback capacitor is 1.3%.

A simplified front-end schematic is shown in Figure 5.7 for explanation of the accumulation tests. Transistors driven by Φ are half-sized dummy devices,



(a)



(b)

Figure 5.6: Measured charge injected per accumulation plotted versus the pixel signal voltage. (a) shows results from the modified pixel and (b) shows results from the original pixel (see section 4.2.1). The front-end feedback capacitance is differentiated by symbols and was given as □: C_F = 300 fF, △: C_F = 466 fF, ∗: C_F = 500 fF, ○: C_F = 1666 fF. A positive injected charge induces the same polarity output change as signal from detected x-rays.

transistors driven by $\overline{\Phi}$ are actual switches. A procedure to accumulate onto C_{F1} and C_{F2} proceeds by first closing all switches to clear charge across C_{F1} and C_{F2}. $\overline{\Phi_{F1}}$ and $\overline{\Phi_{F2}}$ are then opened. $\overline{\Phi_F}$ is then opened. Next, $\overline{\Phi_{F1}}$ is closed to begin ex-

posure onto C_{F1}. To end exposure $\overline{\Phi_{F1}}$ is opened. Then $\overline{\Phi_F}$ is closed to reset the front-end and to act as a shutter for incident signal. $\overline{\Phi_F}$ is then opened. Next, $\overline{\Phi_{F2}}$ is closed to begin exposure onto C_{F2}. To end exposure $\overline{\Phi_{F2}}$ is opened. This completes a single accumulation onto both C_{F1} and C_{F2}. A dummy-switch was not included on the right side of switches $\overline{\Phi_{F1,2}}$ since that node is high impedance and it was assumed that charge injected in one operation would be removed in the next operation. This omission could be the cause of the signal dependence of the charge injection. However, parasitics from the circuit layout could also be the cause of signal dependence.

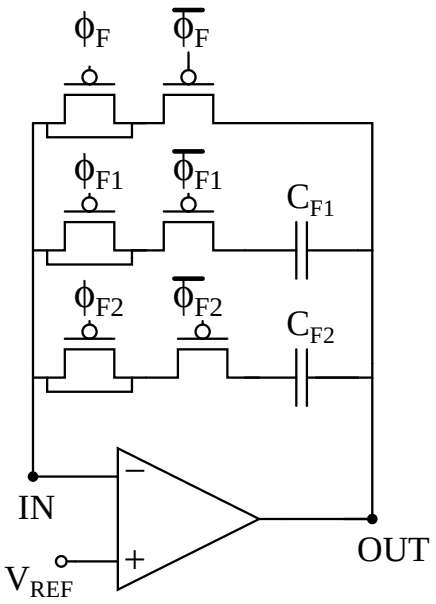


Figure 5.7: Front-end schematic simplified for discussion of accumulation tests. Φ and $\overline{\Phi}$ are complementary clocks.

It is instructive to compare the measured charge injected per accumulation with that anticipated from calculations. A single PMOS switch at the front-end measured 1.44×0.36 μm with a multiplicity of two. The charge injected per operation is given by the clock-feedthrough: $Q_{CK} = \Delta V_{CK} W C_{ov}$ and the channel charge injected: $Q_{CH} = WLC_{ox}(V_{DD} - V_{IN} - V_{THP})$, where $C_{ox} = 4.9\,\mathrm{fF}/\mu\mathrm{m}^2$ is the

gate-oxide capacitance, $C_{ov} = 0.22\,\text{fF}/\mu\text{m}$ is the gate-drain and gate-source overlap capacitance, $V_{THP} = 0.6\,\text{V}$ is the threshold voltage, and V_{IN} is the voltage at the transistor source. Without considering the dummy switches the charge injected per operation is estimated to total 5 fC for each switch. Per accumulation there are three switch operations that inject charge. The results of Figure 5.6 show the experimentally measured charged injection was constrained to less than the worst-case calculations. This suggests that parasitics from the circuit layout are not a significant source of the charge injected. A reduction of the signal dependence of the charge injected per accumulation may be possible with a more complex approach to the switched capacitor circuit. But section 5.5.2 will demonstrate a successful correction procedure for the injection, which may dissuade attempts to reduce the charge injected by addition of more complex circuitry. Note that $C_F = 1666\,\text{fF}$ engages three feedback capacitors in parallel and has three switches that inject charge.

5.5.2 Accumulation calibration

The dependence of the charge injected per accumulation upon the signal integrated introduces a source of non-linearity in the pixel response that can be corrected. For many experiments subtraction of a dark image with the same number of accumulations will sufficiently remove the charge injected per accumulation. When more accuracy is desired, one approach to extract a measure of the incident signal intensity considers the pixel output voltage to follow a recursion relation:

$$V_{n+1} = V_{sig/acc} + \frac{dV}{dn}(V_n), \tag{5.1}$$

where n is the accumulation number, $V_{sig/acc}$ is the x-ray signal per accumulation, and $\frac{dV}{dn}(V_n)$ is the measure of charge injected per accumulation as a function of

pixel voltage, which was represented as a fifth-order polynomial function of V for the correction technique. The desired result is the measure of the incident signal $V_{sig/acc}$, which is assumed constant during acquisition. The detector measures V_N, where N is the total number of accumulations. To find $V_{sig/acc}$ an initial guess of $V^{g1}_{sig/acc} = (V_N - V_1)/N$ is made and the recursion relation of equation 5.1 is evaluated to find V^{g1}_N. The new value of V^{g1}_N is used to update the guess for $V_{sig/acc}$. The iteration continues to step r until $V^{gr}_N \approx V_N$.

In practice, the technique to correct for charge injection per accumulation may not be needed when the signal level is low. In this case the injected charge per accumulation can be removed by subtraction of a dark image acquired with the same number of accumulations since the signal level for both will be similar.

To test the correction technique and the calibration curves acquired with the in-pixel charge injector a data-set was taken with a constant laser spot attenuated 1000-fold incident on the detector with varying numbers of accumulations. Each accumulation integrated signal for $4\,\mu$s. Shown in Figure 5.8 is the integrated signal in the spot versus the number of accumulations with and without the calibration technique applied measured by four front-end feedback capacitances. The lines are linear fits to the data. The norm of the residuals of the linear fits are 12.0, 8.5, 8.8, and 11.5 for the corrected data and 81, 356, 271, and 262 for the uncorrected data with, respectively, feedback capacitances of 1666, 300, 466, and 500 fF. The correction technique collapses the four raw curves (magenta) into nearly indistinguishable curves (blue) and improves the linearity of the integrated value measured versus the number of accumulations.

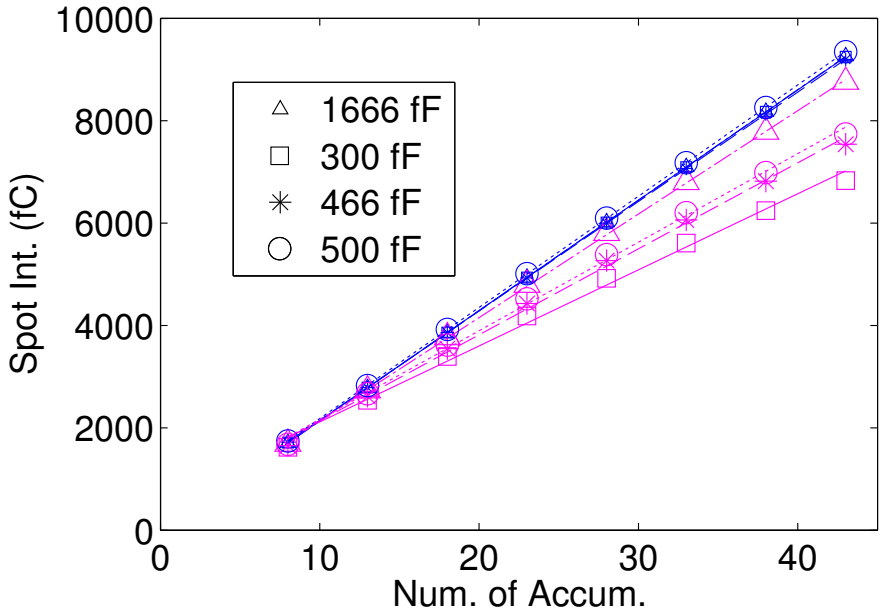


Figure 5.8: Comparison of the integrated intensity in a fixed intensity laser spot (Spot Int.) measured using the accumulation functionality versus the number of accumulations (Num. of Accum.) with (blue) and without (magenta) application of the correction technique. Lines are linear fits. The size of the spot integration region was 42 pixels.

5.5.3 Noise

The noise per accumulation was studied for multiple values of feedback capacitance. The noise measured was differentiated into two sources by fits to the form $\sigma(N)^2 = \sigma_F^2 + N\sigma_{acc}^2$, where σ is the total noise measured, σ_F is the fixed read-noise, σ_{acc} is the noise added per accumulation, and N is the number of accumulations. This measurement was acquired using ASICs with and without a companion bump-bonded detector layer. The bump-bond and detector layer add capacitance to the pixel front-end and increase the reset noise added per accumulation. The measurements are shown in Figure 5.9 with lines overlayed that follow the form $(\sqrt{kTC_F}) + \sqrt{kTC_{IN}})/C_F$. The accurate correspondence between the measurement and the $\sqrt{kTC}$ expression confirms that the accumulation noise arises from capacitive reset noise at the front-end. Table 5.3 shows

the fixed read-noise and noise per accumulation extracted from the data fits from the modified half of a hybridized detector. Also shown is the number of accumulations possible before the added accumulation noise matches the fixed read-noise.

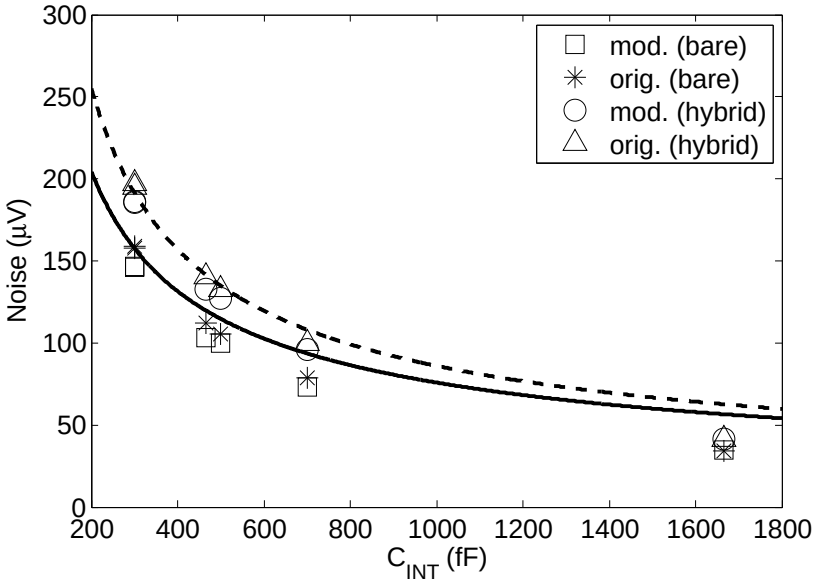


Figure 5.9: Noise growth per accumulation plotted for different values of the front-end integration capacitance. Lines follow the form of $(\sqrt{kTC_F} + \sqrt{kTC_{IN}})/C_F$ with $C_{IN} = 40\,\text{fF}$ and $C_{IN} = 130\,\text{fF}$ for solid and dashed lines, respectively. Data is shown for a hybridized detector (hybrid) and an ASIC without a bump-bonded detector (bare) and is differentiated by modified (mod.) and original (orig.) ASIC halves.

Table 5.3: Noise measured from accumulations differentiated as fixed read-noise and noise per accumulation. The fourth column shows the number of accumulations possible before accumulation noise matches the fixed read-noise.

C_F (fF)	σ_F (μV)	σ_{acc} (μV)	N for $\sigma_F^2 = N\sigma_{acc}^2$
300	550	186	9
466	496	133	14
500	490	127	15
700	473	96	24
1666	452	42	117

5.5.4 Accumulation demonstration

The accumulation functionality allows measurement of a repetitive signal with less noise than other methods (see the fourth column of Table 5.3). To demonstrate this the detector was illuminated with a laser spot modulated with a sinusoid at 25 kHz. The light intensity was attenuated by 10,000 using a neutral density filter for low signal level imaging (Coherent Laser, Santa Clara, CA, Lab Laser MVP/VLM2). Four accumulation elements captured the intensity at four phases of the oscillation: 0°, 90°, 180°, 270° with the laser at full intensity at 90° and off at 270°. Two methods of imaging this scene were compared. One technique captured each phase of the oscillation once with an exposure time of 200 ns and then the image was read out. Fifteen of these images were averaged to form a composite image. The second technique used the four accumulation elements to capture each phase of the oscillation with a 200 ns exposure time fifteen times before the detector image was read out. For this second technique, the measurement was calculated from one single image rather than an average. In both cases the total exposure time for the capture of each phase of the oscillation was $15 \times 200\,\text{ns} = 3\,\mu\text{s}$. The first technique used post-processing averaging while the second technique averaged in-pixel. The integrated intensity measured, in units of 8 keV x-rays per pixel, along with error-bars of ±one-sigma

are shown in Figure 5.10. In this case the number of accumulations is such that the added accumulation noise is near to that of a single readout. As such the noise increase expected from fifteen image reads compared to a single read and fifteen accumulations is: $\sqrt{15/2} = 2.7$. The ratios of the noise measured were 2.7, 2.4, 2.5, and 3.5, in reasonable agreement with expectations.

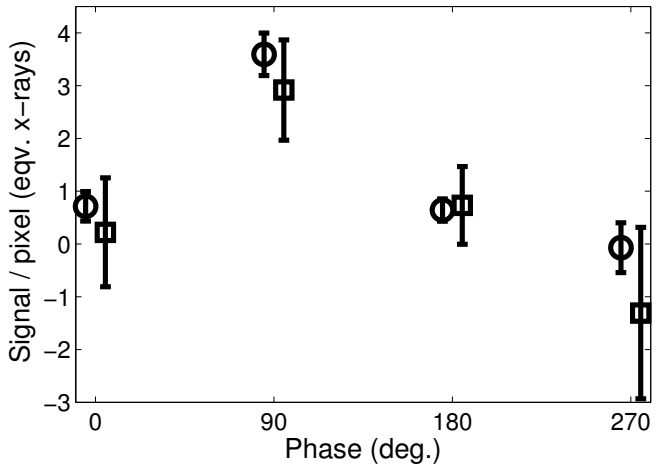


Figure 5.10: Signal per pixel (in equivalent 8 keV x-rays) captured at four phases of an oscillatory stimulus. □ shows data averaged in post-processing. ∘ shows data acquired using the accumulation functionality, i.e. averaged in pixel. The ∘ (□) are offset horizontally by −5° (+5°) for easier visualization.

5.5.5 Spectrum analysis via accumulations

In-pixel accumulation allows the study of fluctuations of the incident intensity at time-scales beyond the detector readout time. Imagers without such a functionality are not able to unambiguously detect frequencies greater than half the inverse of the detector readout time. To demonstrate detection of frequencies far beyond the readout time the PAD was illuminated by a laser (Newport Corp., Irvine, CA, Model LQA635-03C) modulated by a sinusoid at a frequency of 300 kHz ($T_{MOD} = 3.33\,\mu$s) and the light intensity was attenuated by a factor

of 1000. The detector was configured to accumulate into two of the front-end feedback capacitors with ten accumulations acquired by each before readout (the detector was not synchronized to the laser modulation). The sum of the exposure time for each accumulation and the time between accumulations, T_{PER}, was varied from 150 ns to 96 μs with a duty-cycle of 20% for each accumulation element. Fifty images were readout at each fixed setting of T_{PER}. A schematic of this acquisition configuration is shown in Figure 5.11.

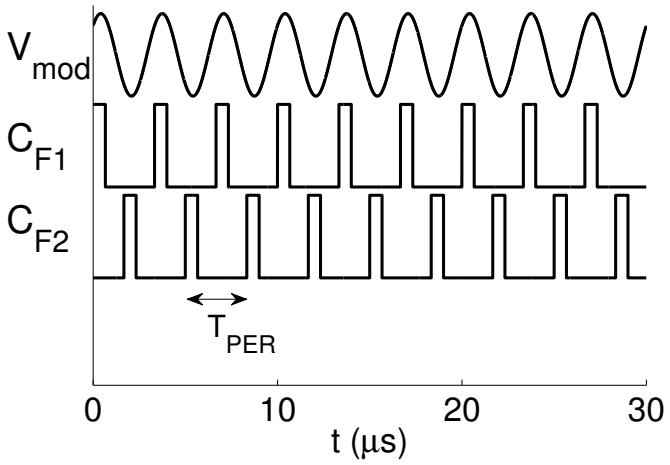
The transfer function of the front-end integrator has a low-pass characteristic, which was exploited to avoid aliasing by maintaining a constant duty-cycle at each T_{PER}. In other words, the exposure time was adjusted to be a constant percentage (20%) of T_{PER}. The power spectral density was estimated as the magnitude of the difference of the two accumulation elements divided by their sum:

$$PSD(T_{PER}) = \sum_{n=1}^{N} \left(\frac{|I_{F1,n}(T_{PER}) - I_{F2,n}(T_{PER})|}{|I_{F1,n}(T_{PER}) + I_{F2,n}(T_{PER})|} \right), \tag{5.2}$$

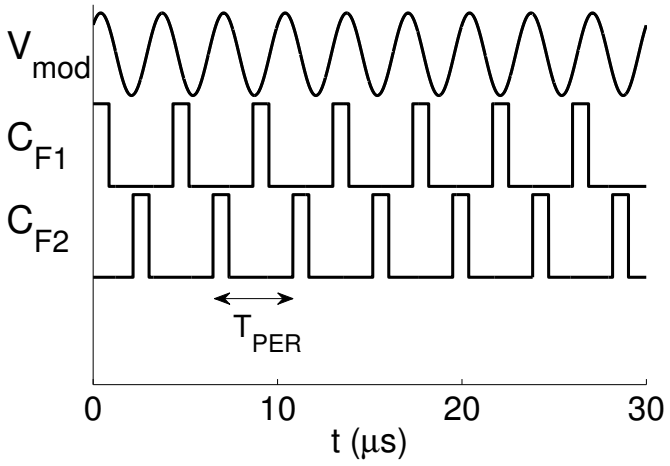
where $I_{F1,n}$ is the intensity measured by accumulation element 1 in image n, and $N = 50$ is the total number of images acquired.

The results are shown in Figure 5.12. The dominant frequency extracted was $f_0 = 300$ kHz, which was the modulation frequency. The dominant sub-harmonics measured were at $f_0/3, f_0/7, f_0/11$. The relation between the control voltage and laser output is not linear [129], which is the expected source of the $2f_0$ harmonic signal and its sub-harmonics at $2f_0/3$, $2f_0/7$, and $2f_0/11$. The difference calculation of equation 5.2 implies that only odd sub-harmonics will be detected. The absence of the sub-harmonic at $f_0/5$ is anticipated since the duty cycle of 20% gives an exposure time equal to the period of modulation for $T_{PER} = 5T_{MOD}$. The duty-cycle is an important parameter that determines the magnitude of sub-harmonics detected.

Figure 5.12 is a simple demonstration to access frequencies beyond the de-



(a)



(b)

Figure 5.11: Explanation of the imaging configuration used to extract power spectral density (PSD) of the incident intensity. The top sine-wave trace shows the signal that modulated the laser source. The middle trace shows the acquisition windows for C_{F1} and the bottom shows the same for C_{F2} (a high level integrates signal). C_{F1} and C_{F2} are $\pi/2$ radians out of phase. (a) shows the example for a T_{PER} that matches the frequency of laser modulation so that the acquisition windows and the modulated incident intensity remain coherent throughout the acquisition, which will result in a high measured PSD. (b) shows an example for a T_{PER} where the exposure windows and intensity modulation are at different frequencies and so coherence is lost. In this case the measured PSD will be less. The schematic is truncated at 30 μs but in actuality continued for ten accumulations in both C_{F1} and C_{F2}.

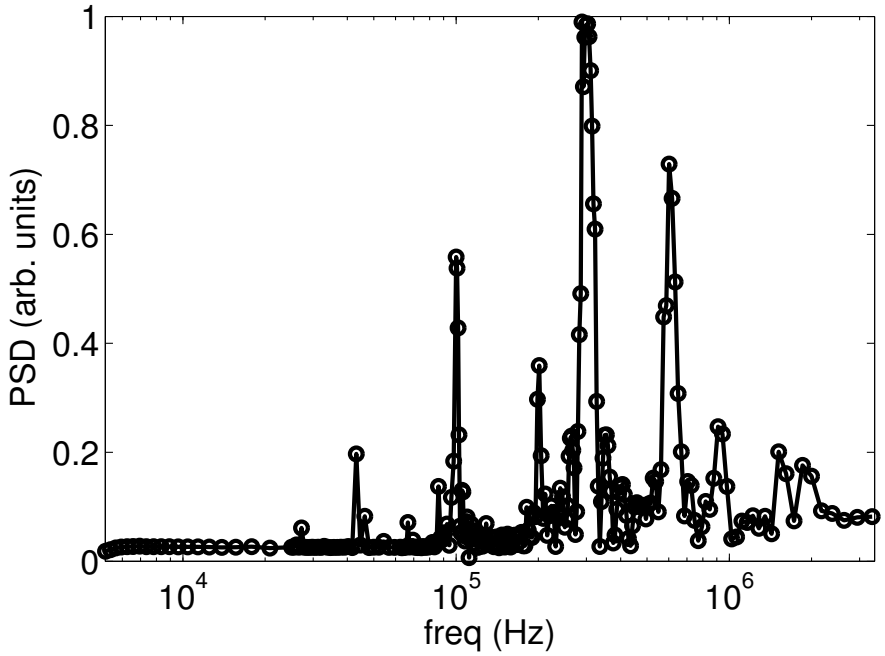


Figure 5.12: Measured intensity power spectrum of a laser modulated at 300 kHz.

tector readout time. This idea simply scratches the surface of the new imaging modalities possible with the accumulation functionality. For example, the presented method to extract the intensity power spectral density could be used for x-ray photon correlation spectroscopy (XPCS) experiments as discussed in section 1.1.2. The desired measurement of XPCS experiments, the intensity autocorrelation function, is related to the power spectral density by a Fourier transform (Wiener-Khinchin theorem) [130]. As such, the PSD estimation technique described above could be another way to study the fluctuations of a sample with XPCS. This approach could be particularly advantageous for samples that fluctuate in microseconds or less studied with highly coherent x-ray sources such as the proposed Energy Recovery Linac (ERL). A photon counting approach would be limited by Poisson statistics in signal-to-noise at microsecond timescales whereas, the analog integrating approach presented above does not have such a flux-rate limitation. XPCS experiments are often photon limited, so if an

accumulating PAD were designed for XPCS an increase of the PAD front-end charge to voltage gain to reduce the detector read-noise may be prudent.

5.5.6 Accumulation conclusions

Accumulation was added to analog integrating PADs so that the signal may be brought above read-noise or Poisson noise before read out. Effectively this technique provides a way to increase the exposure time without smearing time resolution. Further, since accumulation allows acquisition at time separations shorter than the readout time, low-frequency noise contributions from incident intensity fluctuations of the x-ray beam may be reduced.

5.6 Radiation hardness

Radiation robustness was evaluated by dosing a bare ASIC held at -24 C at a rate of 2 Gy(Si)/sec. X-rays were produced by a rotating anode source operated at 40 kV and 50 mA (Enraf Nonius, Model FR571, Bohemia, NY) with multilayers to select 8 keV radiation (Osmic model CMF15-165Cu8, Troy, MI). An exposure time of 1 s was sufficient to detect the incident x-rays and confirm the location of the x-rays on the chip. An area in the center of the chip of 1.2×1.2 mm^2 was dosed.

The chip was irradiated to levels of 5, 10, 50, 100, 200, 300, 400, 500, and 600 kGy(Si) over the course of three days. With a 500 μm thick silicon detector layer for protection a dose of 600 kGy(Si) at the readout ASIC is reached after exposure to a flux of 3×10^{11} x-rays/s/mm^2 for 94 hours at 8 keV ($\sim$ 800 MGy(Si) at diode layer) or 77 minutes at 12 keV ($\sim$ 5.5 MGy(Si) at diode layer). During dosing images were periodically acquired and the current draw of the power

supply was recorded. Before initial dosing and after each level of dose listed above the x-ray shutter was closed for approximately 35 minutes to perform tests that evaluated chip performance. After the evaluation that followed dosing to 600 kGy(Si), the chip was annealed at 45 °C for 135 minutes and then re-evaluated. The annealing time was limited because the camera system needed to be moved to CHESS. The tests ran and the functionality probed by each were:

- The charge injector was used to test the linear response of the pixels.
- The read-noise and pedestal level were evaluated at multiple exposure times.
- The in-pixel output-buffer was configured in unity-gain and the reference voltage to the non-inverting input was swept.
- Similarly, the unity-gain response of the front-end amplifier was tested.
- The charge injector was used to vary the voltage held on the in-pixel storage capacitors. For each voltage stored the leakage current that discharged the analog storage elements was measured by repeating the experiment at different exposure times. Long exposure times (up to 2 seconds) implied long hold-times and allowed for extraction of storage element leakage current.
- The front-end settling speed of pixels with the 195 fF injection capacitor was tested as in Figure 3.14(a). This experiment injected the equivalent of 4.3×10^3 x-rays of energy 8 keV into a feedback capacitor of $C_F = 1966$ fF.

As expected from dose tests on the first ASIC submission the in-pixel output buffer in the original half of the chip failed after 50 kGy(Si). The results reported below are from the modified half of the chip which remained functional up to 600 kGy(Si).

The static current draw of the chip before dosing was 10.2 mA (the current draw of the support electronics was measured as 26.2 mA without the chip in-place and was subtracted for this measurement). The chip current draw increased to 25 mA after 60 kGy(Si) of accumulated dose. After 60 kGy(Si) of dose the current draw decreased as dose accumulated and reached 17 mA at 600 kGy(Si). After annealing the current draw returned to 10.5 mA. An increase in current draw with accumulated dose was anticipated since the front-end amplifier uses NMOS current sources. As holes accumulate in the gate oxide of the NMOS devices the effective threshold voltage decreases and, subsequently, the current drawn increases. The origin of the decrease in current draw after dosing past 60 kGy(Si) is not understood.

The largest pixel pedestal shift was 8 mV and was found after 200 kGy(Si). The pedestal level returned to pre-dose levels after annealing. This is consistent with results shown in reference [90] where the output pedestal remained relatively constant with accumulated dose up to 13 kGy(Si) at the readout ASIC. This stability, found with a 0.25 μm feature size process, was an improvement over results from the 100×92 PAD (1.2 μm feature size process) which showed considerable shift after 1 kGy(Si) at the redout ASIC. Partly the improvement was due to thinner gate oxides but primarily the improvement is due to a change from a single-ended front-end amplifier (100×92 PAD) to a differential front-end amplifier. Other PADs designed at Cornell in 0.25 μm CMOS have shown less radiation robustness. The in-pixel counter of the MMPAD was found to fail after accumulated dose of ~ 2 kGy(Si). Similarly, the PAD developed for coherent imaging at the LCLS was radiation hard up to an accumulated dose of ~ 2 kGy(Si) [51]. All accumulated dose measures are referenced to the bare readout ASIC.

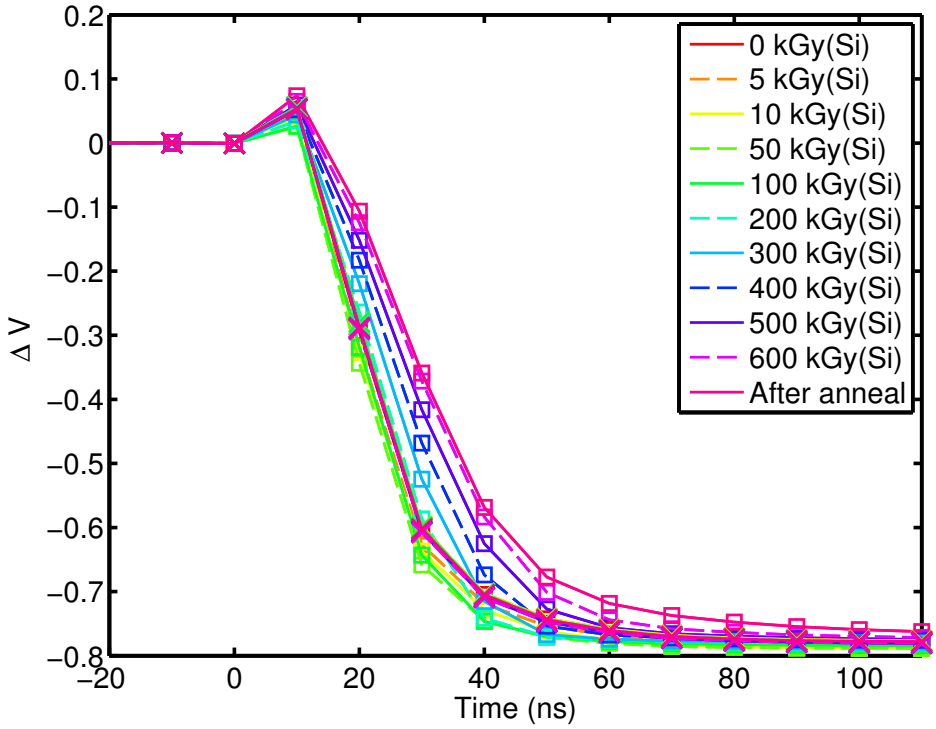


Figure 5.13: High-speed pixel response following an injected charge packet versus accumulated radiation dose. Colors and solid/dashed lines are used to indicate dose level. □ marks traces from the average of four dosed pixels and × marks the average of twelve pixels that were not dosed. The un-dosed curves at different levels of accumulated dose are indistinguishable. The front-end amplifier was biased for a total current draw of 10.8 μA by an un-dosed amplifier.

Tests of the high-speed response of the pixel are shown in Figure 5.13. At low levels of accumulated dose (up to 50 kGy(Si)) the front-end response was found to be faster since the amplifier drew more current. As the accumulated dose increased past 50 kGy(Si) the front-end speed decreased. The response after accumulated dose of 400 kGy(Si) was slowed by a maximum of $\approx$ 30 ns at all dose levels. This reduction in front-end speed may be due to degradation of the transistor small-signal parameters, such as the transconductance. For these measurements a signal equivalent to 4.3×10^3 x-rays of energy 8 keV was injected. A smaller input signal would make the reduction of the amplifier speed

less significant.

The detector read-noise increased by 15% from un-dosed to an accumulated dose of 600 kGy(Si). Annealing removed about half of the dose induced increase in read-noise.

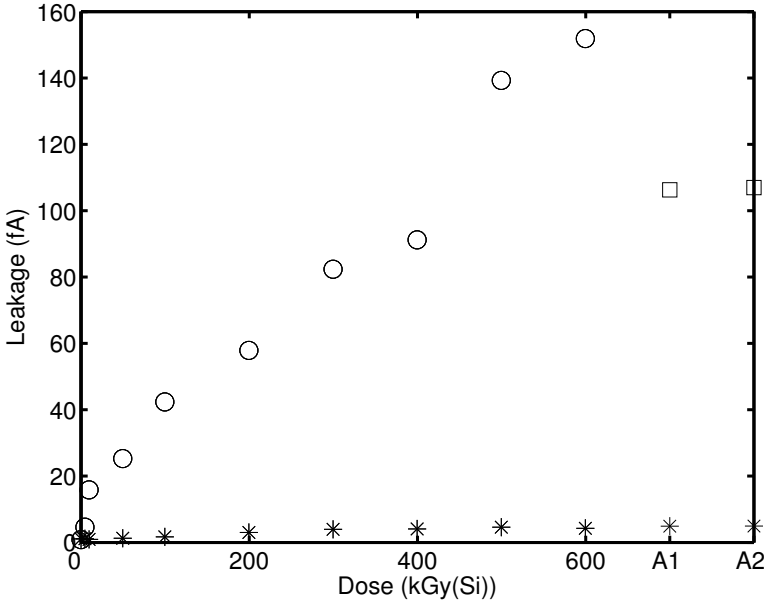


Figure 5.14: Analog storage element leakage versus accumulated radiation dose. Data is from dosed pixels (∘), un-dosed pixels (∗), and dosed pixels after annealing (□). Ticks on the ordinate labeled 'A1' and 'A2' represent two separate measures after annealing. The maximum leakage measured at un-dosed pixels was 4.5 fA.

Figure 5.14 plots the growth of leakage currents that corrupt the analog storage elements versus accumulated dose. Recall that all NMOS transistors implemented as switches were designed with enclosed layout techniques. The leakage remains below 160 fA for all dose levels which confirms that no parasitic edge transistors or field-oxide transistors were activated by dosing. References [118, 119] show the current from field-oxide or parasitic edge transistors to be around nano-Amps or more after dose. From equation 3.23 the measured increase of switch leakage of $\approx \times 40$ could be explained by subthreshold leakage after an NMOS transistor threshold decrease of 120 mV. For a 300 fF storage

capacitor a leakage current of 100 fA implies a droop of 3.3 mV with a readout time of 10 ms, equivalent to the signal from 18 x-ray of 8 keV energy given the lowest front-end gain configuration.

The increase in storage element leakage with dose is the weakest aspect of the radiation hardness of this device. Effects from storage element droop may be subtle and so should be explicitly monitored as dose accumulates. Detector cooling may not be needed to reduce the leakage current from the detector layer due to the short exposure times used for single-bunch experiments (with 100 ns exposure time an average of less than one electron is collected from a detector layer with 100 fA/pixel dark current). However, detector cooling is critical for reduction of the subthreshold switch leakage in the readout ASIC.

Peripheral elements of the readout chip were not dosed. The addressing shift registers were tested versus accumulated dose in the first submission and showed no degradation. The radiation robustness of the analog output multiplexor buffers and of the bias networks was not evaluated. Both were designed using radiation hardened layout techniques. Care should be taken to place these peripheral elements underneath the detector layer for shielding.

5.7 X-ray synchrotron measurements at CHESS G3 hutch

The high-flux x-ray performance of the detector was tested at CHESS G3 hutch. CHESS G-line receives x-ray radiation from positrons via a 49 pole wiggler. X-rays of 8.6 keV energy were selected by a W/B_4C multilayer monochromator with energy bandpass $\Delta E/E = 2.1\%$. G3 receives a flux of up to 5×10^{13} x-rays/sec/mm^2. In the hutch a pair of slits was used to reduce the size of the beam to around 1 mm^2. An aluminum disc with different thicknesses at each position of rotation was used to attenuate the x-ray beam when necessary. A fast

shutter with $\simeq 5$ ms opening and closing times was used to limit x-ray exposure to the detector (Uniblitz/Vincent Associates, Rochester, NY).

The CESR (Cornell Electron Storage Ring) circumference is 768.43 m. At an energy of 5.3 GeV the positrons and electrons travel with a velocity 0.999999995 times the speed of light, which gives a time to circulate the ring of 2.5632 μs. The CESR operator explained that the fundamental frequency of the synchrotron was 11.899034 MHz; the 42nd harmonic of which was the frequency between bunches. The ring was populated with 1281 RF "buckets" for bunches which gives a time for positrons to circulate the ring of

$$\frac{1281}{11.899034 \times 10^6 s^{-1} \times 42} = 2.5632\,\mu\text{s}. \tag{5.3}$$

The rising-edge of the CESR timing signal at a voltage above 1.10 V triggered a pulse-height analyzer/delay generator (Stanford Research Systems, Sunnyvale, CA, Model DSG 535). The delay generator was then used to trigger the PAD. The time from arrival of the synchrotron trigger to release of the trigger to the PAD (referred to as T_D or PAD delay) and the repetition rate of exposures were adjusted with the delay generator. A second delay generator was synchronized to the PAD acquisitions and sent an opening pulse to the fast x-ray shutter. The shutter was opened for 10 ms to up to 50 ms depending on the experiment.

The detector layer was biased to 290 V. The detector temperature was stabilized with a thermoelectric device to temperature of -15 °C for some experiments and -24 °C for others. The detector readout required around 600 μs.

The CESR fill-pattern (distribution of positrons in the storage ring) during this experiment is shown in the schematic of Figure 5.15 and demonstrated with a detector image in Figure 5.16. Five bunch trains circulated the ring with a front-to-front spacing between trains of 280 ns (A in Figure 5.15). In Figure 5.16 the captures of the 2nd and 3rd trains contain more signal than that of the 1st,

4th, and 5th trains. The fill-pattern had six bunches in the 2nd and 3rd trains and five bunches in the other trains. For the acquisition of Figure 5.16, the detector measured an integrated intensity of 1.75×10^5 x-rays for the two bright trains and 1.44×10^5 x-rays for the other trains (a ratio which approximately matched that of the number of bunches: $1.22 \cong 6/5$).

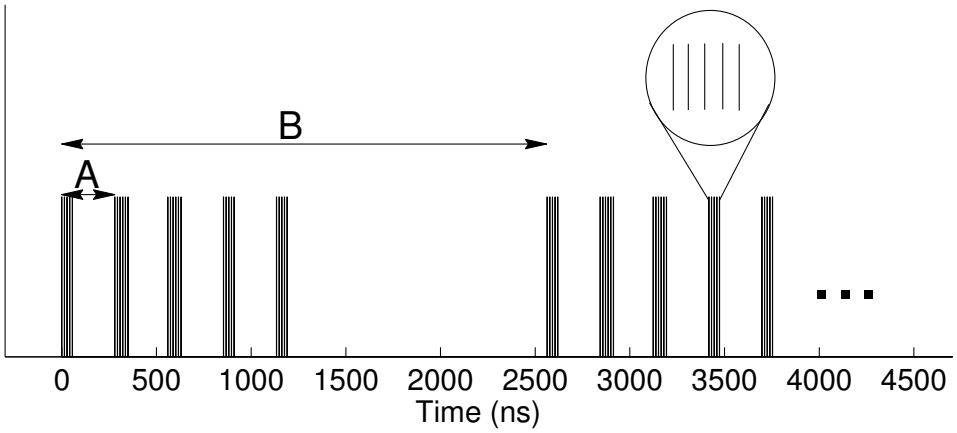


Figure 5.15: The positron fill pattern at CHESS during the synchrotron run. Each individual vertical bar is a bunch of positrons. The graph shows five trains of bunches as each circulates the synchrotron ring twice. The trains, from left to right, are referred to as 1-5. Trains 2 and 3 had six bunches and trains 1, 4, and 5 had five bunches. The front-to-front train spacing was 280 ns (labeled by A). The time for a train to circulate the synchrotron ring was 2563.2 ns (labeled by B). The time between bunches in a train was 14 ns.

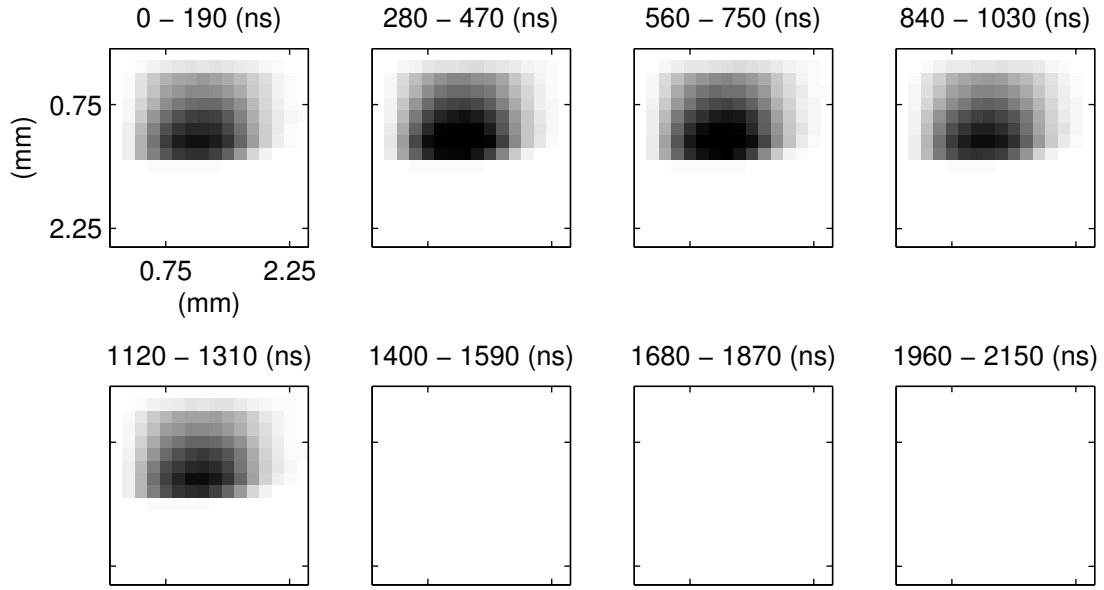


Figure 5.16: A single image recorded at CHESS to illustrate the fill pattern. The linear gray-scale is set from -1 x-ray (white) to 3.7×10^3 x-rays (black). The image shows the output from all eight in-pixel storage elements with the time-window, 190 ns in duration, covered by each in-pixel storage element labeled above the image. Time-window 0-190 ns captured train 1, trains 2-5 were captured in the next successive time-windows, and the last three time-windows captured the period without x-rays (1200 - 2560 ns in Figure 5.15). The sharp edge at the bottom of the spot is hypothesized to be due to vignetting from upstream optical elements.

5.7.1 Settling speed

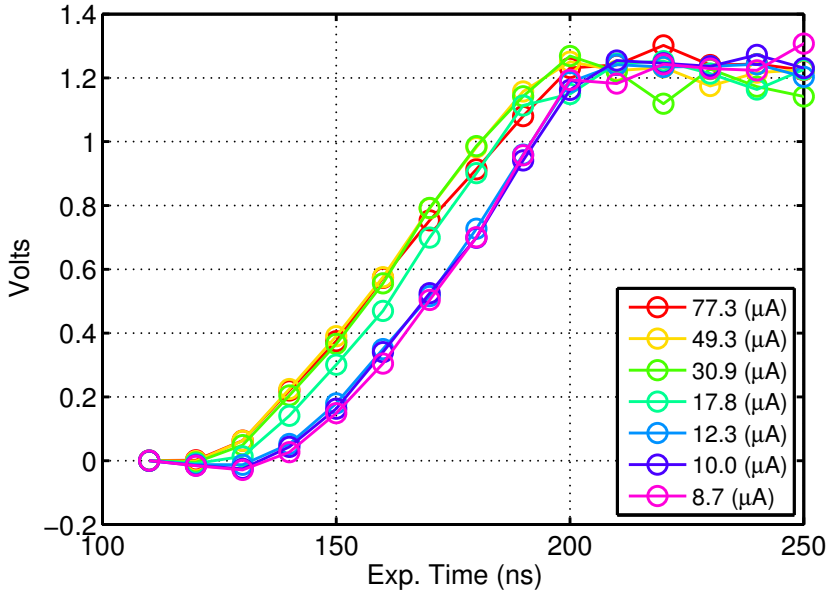
Pixel settling was studied versus the exposure time by acquisition of signal from the fifth train. The interval of 1160 ns between the fifth train and the first train allowed for expansion of the exposure time past the time needed for complete settling without arrival of another train. Figure 5.17 shows the output from a single pixel versus exposure time for different levels of front-end amplifier bias. The PAD delay was timed so that x-rays did not arrive in the shortest exposure time of 110 ns. Figure 5.17 (a) shows acquisitions with C_F = 700 fF and (b) shows acquisitions with C_F = 1966 fF. The data was normalized for slow drifts in beam

intensity using measurements from the ion chambers. Faster beam intensity fluctuations at ≈ 100 Hz were not removed. These fluctuations are quantified and discussed later in the Section 5.7.3. Most likely, these fluctuations are the cause of the variations in the fully-settled values at exposure times > 180 ns.

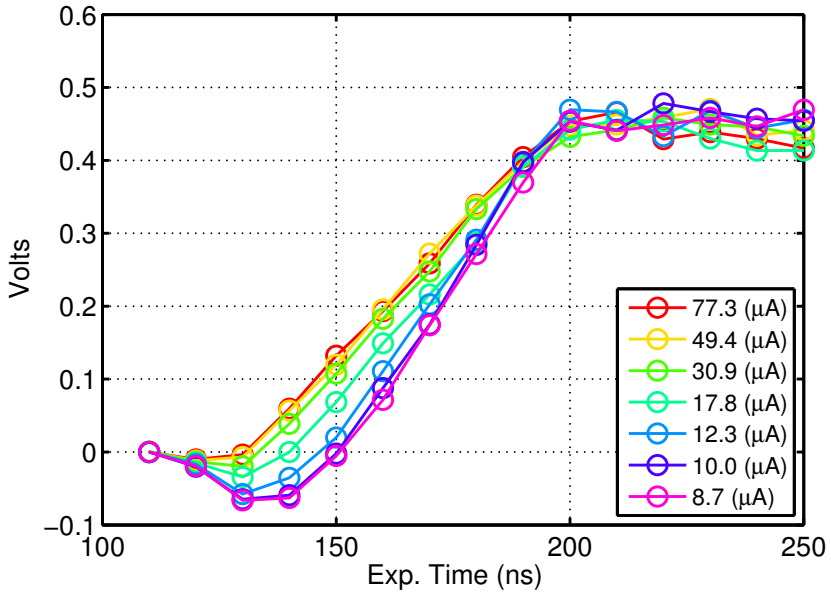
The temporal length of the fifth train was 56 ns and the hole collection time for the 500 μm thick, assumed as 7.5 kΩ·cm resistivity, silicon detector layer is calculated as 22 ns. Both of these effects need to be deconvoluted from the curves in Figure 5.17 to extract the response of the front-end amplifier. X-rays first arrived at the detector at the end of the 120 ns exposure. Signal collection was complete at exposure end for exposure times greater than 200 ns, which shows that the speed was primarily limited by the x-ray duration and charge collection from the detector layer. Capacitive feed-through of the input signal to the output (equation 3.10) before the amplifier responds is noticeable in Figure 5.17(b) at exposure times 130 and 140 ns and most pronounced for low amplifier bias.

For Figures 5.17 (a) and (b) the total signal acquired by the pixel was 880 fC, equivalent to around 2300 x-rays of 8.6 keV energy. The charge deposited and duration of the signal current (78 ns) implies an instantaneous per pixel photocurrent of 11.2 μA for this experiment.

The capacitive configuration used in Figure 5.17 (a) gives a capacitance to slew of C_{slew} = 417 fF from which it is estimated that a current to the load of 7.6 μA was supplied for all bias levels. The amplifier configured at the lowest total dissipation of 8.7 μA implies 8.7 μA/6 = 1.45 μA current to the load in static operation (1/6th of the total current is dissipated in the output branch). Thus, the class AB operation of the front-end amplifier is verified in Figure 5.17(a) as the current to the load in the slewing situation is greater than the static current



(a)



(b)

Figure 5.17: Settling of the signal from the fifth train versus exposure time acquired at different levels of front-end amplifier bias current. The trace is the output of a single pixel. (a) shows the data acquired with C_F = 700 fF (b) used C_F = 1966 fF. The legend indicates the total static current drawn by the amplifier. For both figures the total signal acquired by the pixel was around 2300 x-rays; the data is shown in volts to allow for quick calculations of slew-rate.

to the load.

The minimum exposure time of the detector is not demonstrated by Figure 5.17. The exposure time needed to fully measure the signal of the train in Figure 5.17 is larger than the minimum possible exposure time because the PAD is triggered with respect to the synchrotron bunch structure so that the x-rays arrive at the end of the exposure with 120 ns exposure time. Once the x-rays arrive the signal persists for 56 ns since the train consists of five bunches. The time from x-ray arrival to the plateau at an exposure time of 200 ns was 80 ns, which suggests that the response time is dominated by the sum of the hole collection time and the duration of the x-ray signal and is not slowed significantly by the pixel.

5.7.2 Bunch train resolution

An experiment was performed to resolve the individual bunch trains as in Figure 5.16. To do so, the PAD exposure time and time between frames was set to 190 and 90 ns respectively, so that the sum was the 280 ns interval between trains. The PAD trigger delay (T_D) was adjusted with respect to the synchrotron timing to study the dependence of the PAD response to the time within the exposure window that the x-rays arrived. Shown schematically in Figure 5.18, as the PAD trigger delay was increased the x-rays arrived earlier in the exposure window.

Figure 5.19 shows the output of each storage element from a single pixel plotted versus the PAD delay. The first group of peaks show that C_{S2}, C_{S5}, and C_{S6} measured the lower intensity bunch trains (1, 4, and 5); C_{S3} and C_{S4} measured the high intensity trains (2 and 3); and C_{S1}, C_{S7}, and C_{S8} were not illuminated. The duration of the rising and falling edges and the flat-tops of the

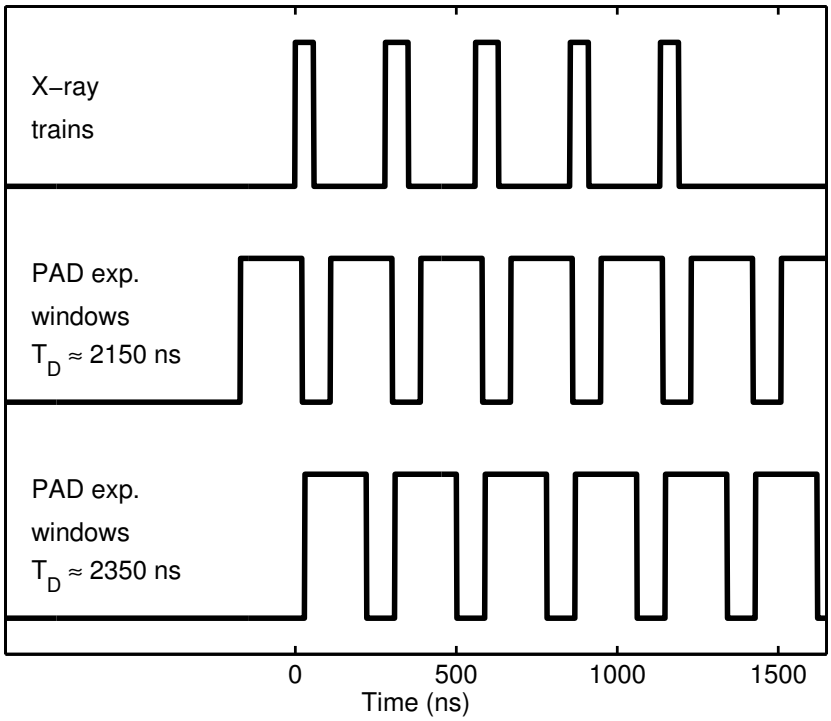


Figure 5.18: A schematic to explain the shift of the PAD exposure windows as the PAD trigger delay (T_D) was adjusted. A high-level in the top trace indicates the x-ray trains. Exposure windows are indicated by a high-level. The middle trace shows a PAD delay such that the x-ray signal from train 1 was captured near the end of the exposure time of the first storage element. In the bottom trace the PAD delay was advanced 200 ns so that the x-ray signal arrives near the start of the exposure window.

pixel response in Figure 5.19 provide information about the speed of the detector response. For trains with six bunches the rising, flat-top, and falling edge durations were 100 ns, 60 ns, and 100 ns, respectively. For the trains with five bunches the rising, flat-top, and falling edge durations were 90 ns, 75 ns, and 85 ns, respectively. The total time that signal was detected was 250 ns for the five bunch trains and 260 ns for the six bunch trains, which is approximately the sum of the exposure time, x-ray train duration, and the detector collection time.

The results of Figures 5.17 and 5.19 indicate the feasibility of isolation of single bunches with 153 ns spacing at the Advanced Photon Source (APS). The

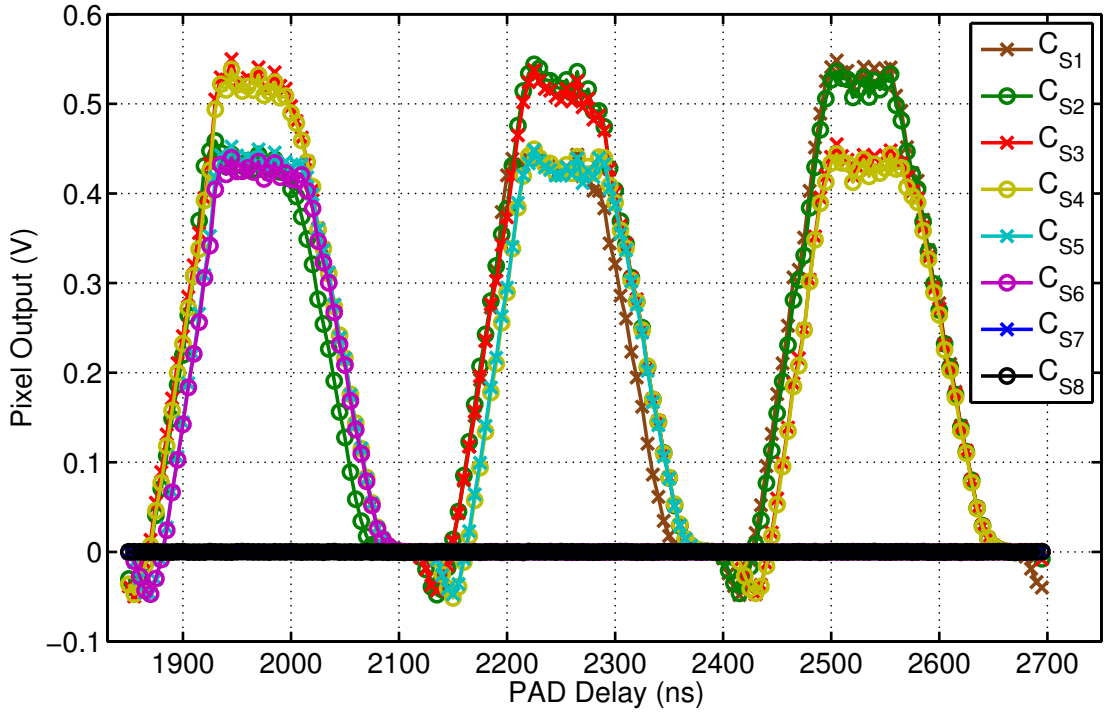


Figure 5.19: Pixel output versus the PAD delay with a train imaged by successive storage elements. The exposure time was 190 ns and the time between frames was 90 ns. C_{S7} and C_{S8} measured around zero at all PAD delays and are indistinguishable in the figure.

flat-top time in Figure 5.19 of 75 ns suggests that at CHESS the entire signal from the train would still have been measured if the exposure time was reduced from 190 ns to 115 ns. Further, at CHESS, the rising and falling edges of Figure 5.19 were slowed by the duration of the trains; at the APS a single bunch, which to the detector behaves as a delta-function signal impulse, arrives every 153 ns. The reduction of the signal duration by 56 ns should allow reduction of the exposure time by at least 25 ns. Therefore, it is estimated that bunches at the APS could be resolved with an exposure time of 90 ns and a time between frames for pixel reset of 60 ns.

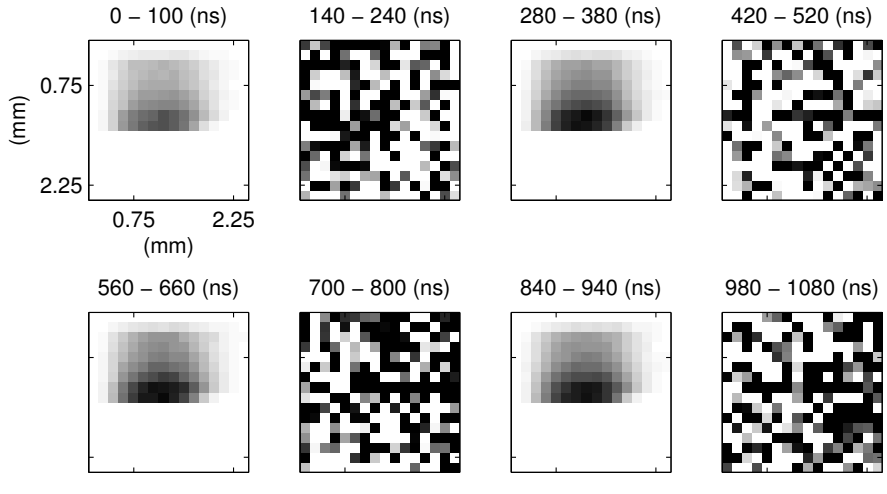
The results shown in Figure 5.19 were used to evaluate the shift of the detector pedestal level and read-noise induced by high levels of x-ray flux. The time-

averaged flux at the brightest pixels was measured to be $4.8{\times}10^3$ x-rays/pix/μs equivalent to $2.1{\times}10^{11}$ x-rays/mm^2/s. At PAD delays of 2550-2600 ns storage elements C_{S5} through C_{S8} should measure zero. The read-noise of these nominally empty storage elements showed an insignificant maximum increase of only 1.2% at the highly illuminated pixels compared to images with the mechanical x-ray shutter closed. The maximum and average integrated signal measured by the highly illuminated pixels in storage elements C_{S5} through C_{S8} were less than $< 0.02\%$ and $< 0.004\%$, respectively, of the signal measured by storage elements C_{S1} through C_{S4} (both of which could be entirely due to noise).

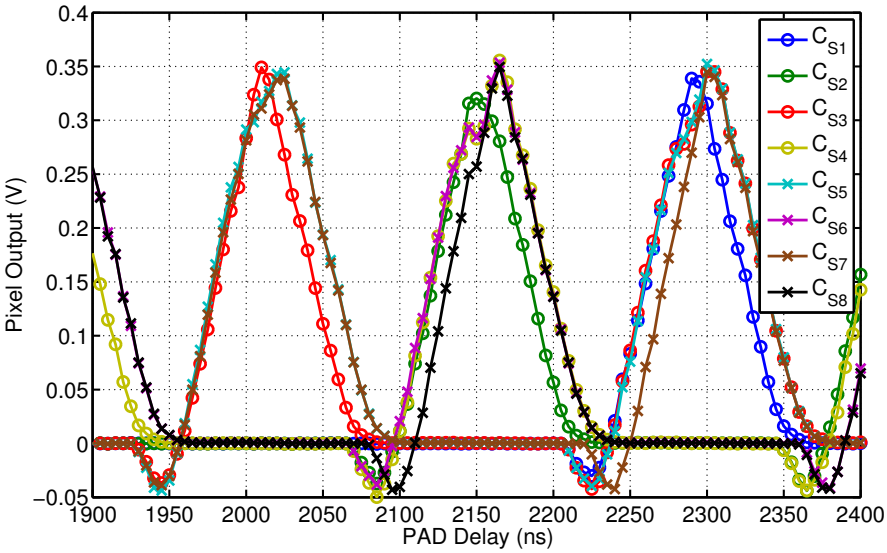
These results on signal-induced pedestal shift and signal-enhanced read-noise seem to be an improvement over the first and second generation microsecond imaging PADs developed in this group [48, 95]. But possibly the difference is a result of measurement technique. Synchronization to the x-ray arrival is important. These results and other tests that measured the pixel output with the front-end amplifier continuously reset suggest that in high-flux experiments the pixel reset switch should not be released nor should the front-end output be latched within $\approx$30 ns after the arrival of a bunch.

To test the limits of the detector response speed the PAD was configured with an exposure time of 100 ns and a time between frames of 40 ns to image a train with every other storage element of the pixel. Isolation of x-ray signal into every other PAD storage element is not necessary for experiments but was tried as a demonstration. An average image acquired with a PAD delay of 2320 ns is shown in Figure 5.20(a). The odd numbered storage elements captured a train with an integrated signal of 5.2×10^4 x-rays. The even numbered storage elements do not show residual signal from the x-ray illumination. Figure 5.20 shows the output from a bright pixel versus the PAD delay. The curves do not

show flat-tops which implies that complete signal acquisition was not achieved. The curve fall- and rise-times are limited by the duration of the x-ray trains and the detector layer hole collection time.



(a)



(b)

Figure 5.20: (a) An average of twenty-four images recorded at CHESS with a train imaged by every other storage element. The linear gray-scale is set from -2.7 x-rays (white) to 2.7 x-rays (black) in the empty storage elements (140-240, 420-520, 700-800, 980-1080 ns) and -1.5 x-rays to 1590 x-rays in the illuminated storage elements. (b) The output from a single pixel versus the PAD delay. (a) shows this data for one single delay time of 2320 ns.

5.7.3 Beam characterization

The x-ray beam in the experimental hutch may have intensity and position fluctuations due to trajectory instabilities of the electron/positron source or from motions of the optics that interact with the x-ray beam. Evaluation of these variations is important, particularly for time-resolved experiments. The capability to diagnose these fluctuations, especially at or exceeding the frequencies of vibrations that may be driven by pumps, is valuable for commissioning of x-ray beam lines.

Conventional x-ray experiments often expose images for seconds, in this case fluctuations much above 1 Hz will be removed by the averaging of the exposure time. Lower frequency intensity drifts can be removed by normalization to intensity monitors such as ionization chambers. These intensity monitors that transmit the x-ray beam are often limited in speed and are not sensitive to position fluctuations. The situation is different for microsecond time-resolved PAD experiments. In this case incident beam fluctuations are not averaged by long exposure times and are not easily monitored. Thus, the x-ray beam must be stable at frequencies approaching MHz otherwise fluctuations may be interpreted as signal.

Devices have been developed as dedicated x-ray beam position and intensity monitors. A monitor that detected beam position fluctuations of around 20 nm at frequencies up to 12.5 Hz was constructed and tested at the Swiss Light Source [131]. The camera system consisted of a 170 μm thick YAG scintillator, a magnifying lens configuration, and a CCD camera with 25 Hz frame-rate. Other work has focused on transparent monitors that track the beam intensity profile while transmitting most of the beam. These devices detect x-rays scattered from a thin amorphous foil with an x-ray camera. The development in refer-

ence [132] used 300 ms exposure times to track the profile of a beam with an intensity of 10^{11} x-rays. Work at Cornell has recently developed an x-ray beam position monitor to use synchrotron radiation as a measure of electron beam position in the storage ring with implications for the damping rings at the International Linear Collider [133].

The readout time of the PAD camera and the ability to resolve signals on sub-microsecond timescales allowed for unique characterization of the x-ray beam on microsecond time-scales. Since the PAD directly images the beam on an array of pixels the beam profile is extracted, which provides more diagnostic information than four-quadrant type beam position monitors. The in-pixel storage allowed for study of temporal correlations of a train sampled at each pass around the synchrotron ring. This characterization of the temporal evolution of the position and intensity fluctuations of the x-ray beam is valuable for future time-resolved experiments at CHESS.

In this experiment the PAD imaged train five from the synchrotron with all eight in-pixel storage elements. The temporal separation between the capture of train five by each storage element, ΔT, was varied to study the time correlation of the position and intensity fluctuations. Since the time for the positron trains to circulate the ring was 2.56 μs (B in Figure 5.15) with ΔT = 2.56 μs each successive storage element captured train five after a single pass around the ring. ΔT = 5.12 μs implies that the train circulated the synchrotron ring twice between the image captured by C_{S1} to the image captured by C_{S2}. Each image measured the x-ray signal at multiple time differences, τ, from ΔT, $2\Delta T$, ... to $7\Delta T$, because of the eight in-pixel storage elements. The time between PAD images was limited to a minimum of 700 μs by the readout time and varied from 719 μs to 2.7 ms to extract a range time correlations.

The intensity, I, was measured as the sum of the entire spot; horizontal and vertical positions were found with a center-of-mass algorithm. To study the fast timescales extracted by the in-pixel storage elements, intensity and position time correlations were evaluated by calculation of the average RMS deviation versus the time difference, τ, between the measurements. Fractional intensity deviations are evaluated as

$$FDEV_I(\tau) = \frac{\sqrt{< (I(t) - I(t+\tau))^2 >}}{\sqrt{2} < I >}, \tag{5.4}$$

where <> indicates an average. Positional deviations are calculated similarly, but not normalized to the average position, and indicated as $DEV_X(\tau)$, and $DEV_Y(\tau)$, for horizontal and vertical displacements, respectively. The integrated intensity measured per capture was around 1.1×10^5 x-rays which implies an accuracy limit from Poisson statistics for the measure of integrated intensity of

$$\frac{\sqrt{1.1 \times 10^5}}{1.1 \times 10^5} = 0.0030. \tag{5.5}$$

Figure 5.21 shows the fractional intensity deviations extracted for correlation times from 2.56 μs up to 500 μs. At the shortest correlation times the measurement is close to the accuracy limit set by Poisson statistics. Extraction of a nearly Poisson limited measurement suggests that the accuracy of the detector is maintained at high-flux levels and short exposure times. The linear growth of the intensity deviation with correlation time shows that the integrated intensity from the single train was dominated by low-frequency fluctuations. Consider an intensity of the form $I(t) = A\sin(\omega t)$. The RMS deviation of this intensity is written as

$$DEV_I(\tau)^2 = \frac{A^2\omega}{2\pi}\int_0^{2\pi/\omega} (\sin(\omega t) - \sin(\omega(t+\tau))^2 dt \tag{5.6}$$

where the integral averages over all phases of the oscillation. For correlation times much shorter than the inverse of the oscillation frequency ($1/\tau \gg \omega$) the

integral expression is simplified with a Taylor's expansion to

$$DEV_I(\tau)^2 = \frac{A^2\omega}{2\pi}\int_0^{2\pi/\omega}\cos^2(\omega\tau)\tau^2 dt = \frac{A^2\tau^2}{\omega^2}. \tag{5.7}$$

This shows that for an intensity fluctuation that oscillates at a frequency much slower than the correlation times under study the deviation increases linearly with the correlation time.

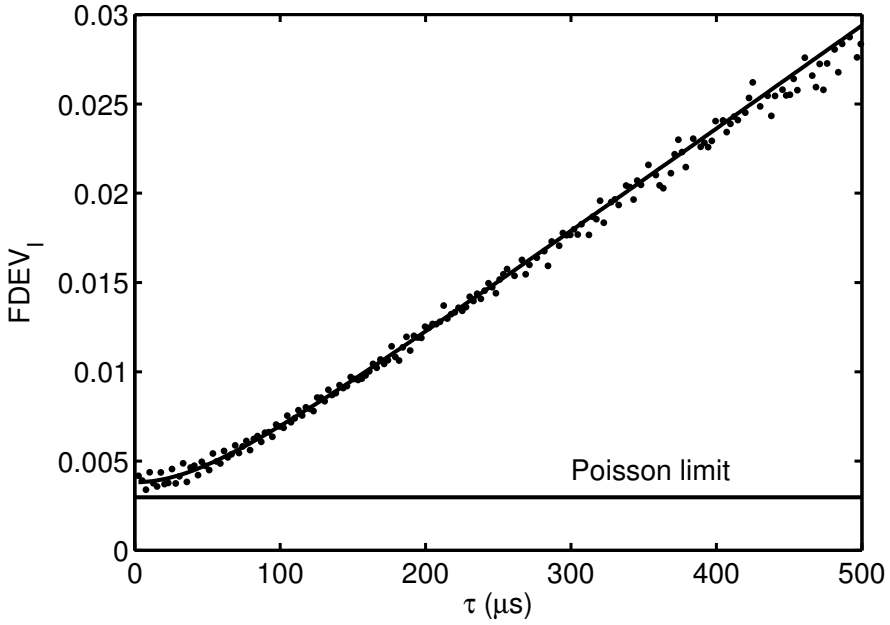


Figure 5.21: Fractional RMS fluctuation of the CHESS G3 beam intensity versus correlation time. The solid-line is a fit $FDEV_I^2 = A(\tau[\mu s])^2 + P$. $A = (5.8 \times 10^{-5}/[\mu s])^2$ and $P = (0.0038)^2$ which shows the limit at short correlation times to be 0.38%.

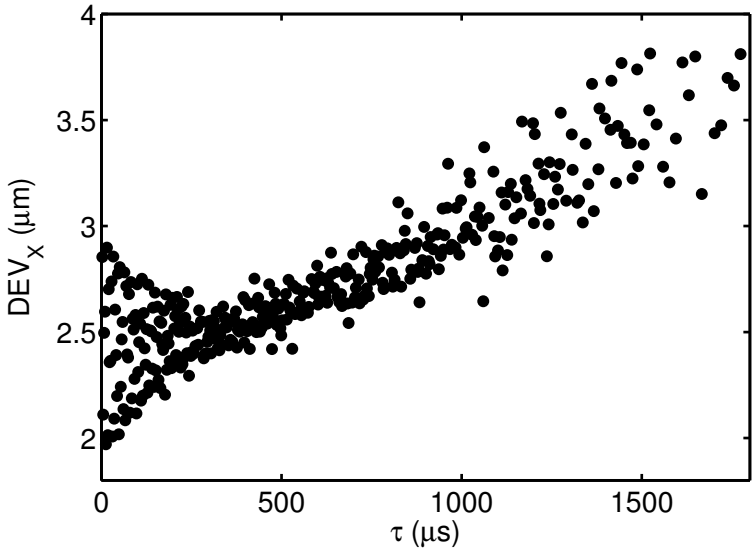
Figures 5.22(a,b) displays the deviations of the center-of-mass of the x-ray intensity in the horizontal direction. Figure 5.22(b) plots the horizontal deviations for correlation times up to 80 μs, which oscillates at a frequency of 163 kHz. The maximum sampling rate of this measurement was limited to the time for the train to circulate the ring. As such, it is not possible to determine if the frequency extracted is the actual frequency or an aliased measure of a higher frequency of the positron cloud motion. The actual possible transverse oscillation frequen-

cies, f, are then $163\,\text{kHz} = |f - N \times 390.1\,\text{kHz}|$ for any integer N. The horizontal x-ray beam motion is hypothesized to originate from betatron oscillations of positron cloud in the synchrotron [134]. The day before these experiments at CHESS began the single beam horizontal betatron measurements were measured by the storage ring operators at a frequency of 227.7 kHz, which would be measured by the PAD as a frequency of $|227.7\,\text{kHz} - 390.1\,\text{kHz}| = 162.4\,\text{kHz}$. These oscillations may be shifted by around a kHz when the ring is populated by both positrons and electrons. To the best of my knowledge no other x-ray detector currently available could make this measurement.

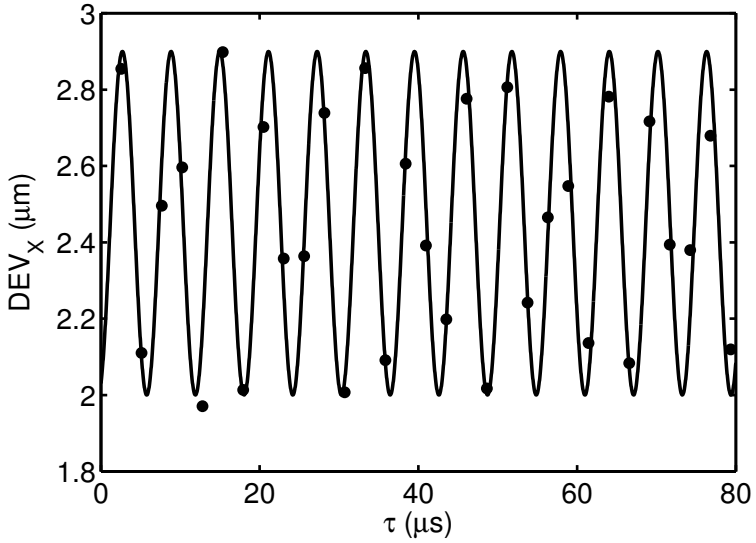
The vertical deviations, not shown, were dominated by low frequency fluctuations (see Figure 5.23).

At timescales accessible by the PAD readout time investigation of the direct time evolution of the beam intensity was possible, as shown in Figure 5.23. The amplitude of these oscillations (almost ±20%) was certainly surprising. A fast Fourier transform (and visual inspection) of these fluctuations revealed the oscillations were at 100 and 200 Hz. After discussion with Dr. Peter Revesz and Dr. Arthur Woll of CHESS, Dr. Revesz measured motions of the G-line monochromator box at frequencies of 98 and 196 Hz using an accelerometer, which were caused by the vacuum pump on the monochromator box. These intensity fluctuations were also seen when the amplified output of an ionization chamber was monitored with an oscilloscope.

Intensity fluctuations in Figure 5.23 would make some time-resolved measurements challenging if not properly accounted for. Fluctuations at 200 Hz could be normalized with ionization chambers as long as the normalization measurements are synchronized to the PAD exposures. The low frequency fluctuations also show that measurements that rely upon correlations between cap-



(a)



(b)

Figure 5.22: Fluctuations of the CHESS G3 beam horizontal position at fast timescales. (a) The top plot shows the horizontal center-of-mass deviations versus correlation times up to 1.8 ms. (b) focuses on the first 80 μs with a superimposed oscillation (solid-line) at 163 kHz.

tures at short time intervals (for example, difference measurements of the in-pixel storage elements) will be less corrupted by incident intensity fluctuations than measures that compare frames separated by detector readout. The high

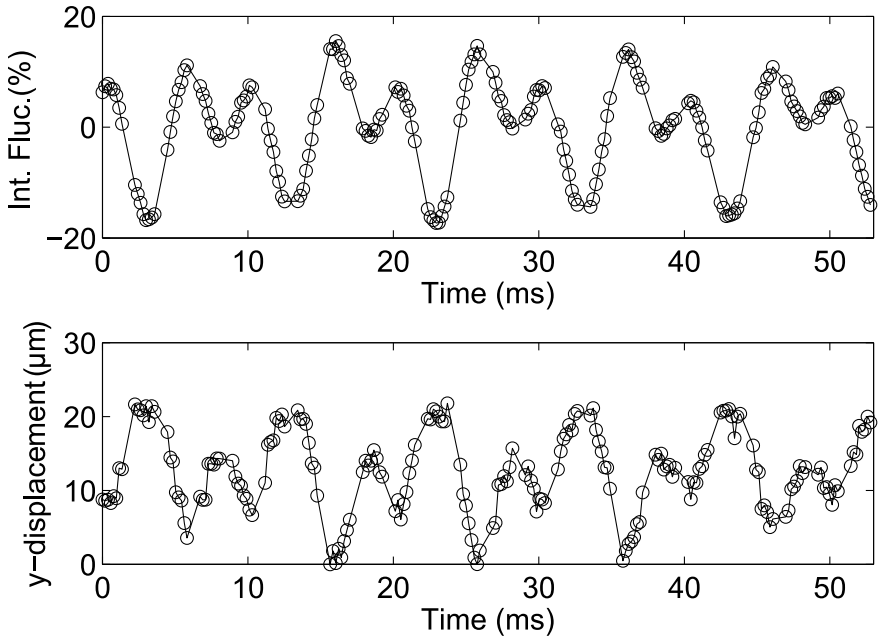


Figure 5.23: Millisecond timescale studies of the beam intensity fluctuations (top) and vertical position (bottom) at CHESS G3.

frequency horizontal deviations are not significant for most x-ray experiments but display extraction of information about the electron/positron beam from synchrotron radiation on a turn-by-turn basis.

5.7.4 Bare ASIC x-ray response

A final experiment at CHESS was used to study the response of a bare ASIC readout chip to high-flux radiation. Ideally, the readout chip is not sensitive to x-rays so that those which penetrate through the detector layer do not create an anomalous signal. However, the transistors in the readout chip may collect x-ray induced charge that can be interpreted as signal. For this experiment, the effects measured were magnified because the readout chip did not have a companion bump-bonded detector layer to absorb incident x-rays. A 500 μm thick silicon detector layer transmits 0.076%, 2.45%, and 32.3% of normally incident

x-rays at, respectively, energies of 8 keV, 10 keV, and 15 keV [135]. The bump-bonds and pad metallizations of the detector chip to readout chip connection will also attenuate x-ray signal but the absorbed fraction is not calculated because of the uncertain thicknesses.

For this measurement (and all the others during the CHESS run) the detector was irradiated during readout. In the case of the bare ASIC, each 10 ms opening of the x-ray shutter provided an estimated 2.6 kGy(Si) of dose to the ASIC; the G3 beam attenuated by only a factor of ×5 was incident onto the bare ASIC (for a flux of $\approx 7.7 \times 10^{10}$ x-rays/pix/s or 3.4×10^{11} x-rays/mm^2/s). Because the original half of the readout chip showed effects from radiation damage early in the experiment all results reported are from the modified half of the chip. These experiments attempted to differentiate the cause of the anomalous signal into three separate sources.

- Signal collected during the exposure time at the pixel front-end. This signal depends upon the exposure time and the value of the feedback capacitor.
- Signal collected after latching a value on a storage element and before readout. This signal increases when storage element hold times are increased.
- Other anomalous signal not readily assigned to the other two categories.

The bare ASIC efficiency for x-ray collection during the exposure time at the front-end was estimated to be 6×10^{-6} (with the same signal polarity as is seen when x-rays are detected with a hybridized device). This is inherently not a problem since a slight change in the efficiency for collection during the exposure time will not change measurement results. Since the 'exposure time' of this anomalous signal is the same as the actual exposure time, in hybridized devices

x-rays that convert in the detector layer will overwhelm signal from x-rays that convert in the readout ASIC.

The efficiency for collection during holding was measured as 2×10^{-6} (with the same polarity as above), with reference to a front-end gain configuration of $C_F = 300\,\text{fF}$. This anomalous effect is deleterious since analog storage elements may be held for times that far exceed the exposure time (for example, a $\sim 10\,\text{ms}$ readout time and a $100\,\text{ns}$ exposure time).

The efficiencies measured for these anomalous effects are reasonably consistent with the collection areas of the sensitive transistors compared to the total area of the pixel. Consider the efficiency for collection at the front-end. For the front-end gain configuration used, a total of 18 transistor diffusions, each with a cross-section area of $1.44{\times}0.72\,\mu\text{m}^2$, may contribute holes to the input. The ratio of transistor diffusion area to pixel area suggests that the collection depth for these experiments was around $0.6\,\mu\text{m}$. This result of a minimal collection depth is encouraging; further, it suggests that benefits from modifications to the CMOS process used, discussed in section 2.5.2, to reduce anomalous collection in the CMOS may be limited. In other words, these results suggest that the charge collected by sensitive nodes of the bare ASIC is highly localized and not from charge that diffuses many microns through the substrate. In this case, CMOS fabrication in an epitaxial process which uses a highly doped bulk substrate that has shorter carrier diffusion lengths than the non-epitaxial process used for this work would not impact the detection efficiency of a bare ASIC.

Due to the anomalous signal collection during storage element holding, high-flux experiments at x-ray energies with limited absorption from the detector layer, may require a mechanical shutter to shield the detector from x-rays during readout. A shutter may also be necessary to mitigate radiation dam-

age to the sample under investigation. Ideally, the shutter would have sub-millisecond opening and closing times.

A negative polarity pedestal shift was also observed that belongs to the third category in the list above. The shift did not depend on the value of the front-end feedback capacitor, the length of the hold-time, the exposure time, or the time the detector waited for a trigger. For the images taken while the x-ray shutter opened this pedestal shift was not seen in the storage elements captured first. The shift varied from 60 to 120 mV, was largest for the storage elements sampled last, and was proportional to the incident x-ray intensity. Most likely this signal originated from x-ray conversion that happened before the exposure. In these experiments the maximum flux specification of 1,000 x-rays/pixel/bunch was exceeded by almost 35. With the incident intensity limited to the maximum flux specification and the detector layer and incident energy chosen for an attenuation of at least a factor of $\times 55$ (500 μm thick silicon at 9.75 keV incident energy) the pedestal shift is anticipated to be less than 100 μV, which is below the detector read-noise.

Future experiments could characterize the anomalous effects from x-ray conversion in the readout chip versus the incident x-ray energy. Higher energy x-rays are transmitted through the detector layer with greater frequency but, subsequent absorption in the sensitive thickness of the readout chip is less likely. Another future experiment could use an x-ray spot focused to around 1 μm diameter to assign the anomalous effects to particular portions of the pixel layout of the readout chip. After setup of a high-flux experiment at x-ray energies with significant transmission through the detector layer a check for anomalous signal with a bare readout chip would be a prudent preparation procedure.

5.7.5 CHESS experiment discussions

The experiments at CHESS showed successful high-speed x-ray measurements with single bunch-train resolution. Lessons were learned that are particularly relevant to experiments at the synchrotron. During these experiments the FPGA master clock was set at 100 MHz. The incoming trigger sent to the PAD was synchronized to the FPGA clock within the FPGA electronics, which set the jitter between arrival of the external trigger and start of the PAD exposure to 10 ns. Experiments that require more accurate synchronization of the synchrotron clock and PAD acquisitions will need reduced trigger jitter. The brute force method would use a faster master FPGA clock, 250 MHz may be feasible, to subsequently reduce the trigger jitter to 2.5 ns. A more elegant technique would phase-lock the FPGA master clock to a harmonic of the synchrotron timing signal.

The edges of Figure 5.19 do not precisely align because of a rounding error that was inherent to timing individual bunches. The temporal bunch separation was not an exact multiple of the 10 ns FPGA timing increments. To eliminate this rounding error the FPGA master clock could be set to a harmonic of the synchrotron clock using the FPGA PLL.

CHAPTER 6

CONCLUSIONS

This chapter presents future developments for the single bunch imaging PAD. The parts from the modified and original ASIC halves that performed best and are appropriate for future fabrications are explained. Possible approaches for design of a detector capable of isolating single pulses at the Cornell Energy Recovery Linac (pulse rate of 770 ps) are presented. Detectors with integrated photodiodes in standard CMOS are an attractive option at low x-ray energy (< 4 keV). At higher energies hybridized devices with ~40 μm thick GaAs detector layers are proposed. Finally, to conclude, the 16×16 PAD camera is compared to other currently available x-ray detectors for single bunch imaging.

6.1 Future Work for Single Bunch PAD

6.1.1 Settling time

Experiments that study the small-signal settling time are presented in order to provide advice on the selection between the modified front-end amplifier or the original front-end amplifier. The experiment used the large injection capacitor to inject 235 fC (equivalent to 665 x-rays of 8 keV energy) into the front-end with a feedback capacitance of C_F = 300 fF. A voltage change of 0.78 V was produced. The time between latching the output signal and the charge injection was swept to create curves similar to those shown in Figure 5.13. The analysis found the settling time constant by a fit to an exponential decay of the values within 40 mV of the final settled values. These results, differentiated by the modified and original half of the ASIC and by a hybridized and a bare device, are shown in Figure 6.1(a). The times for settling to particular levels of accuracy are shown

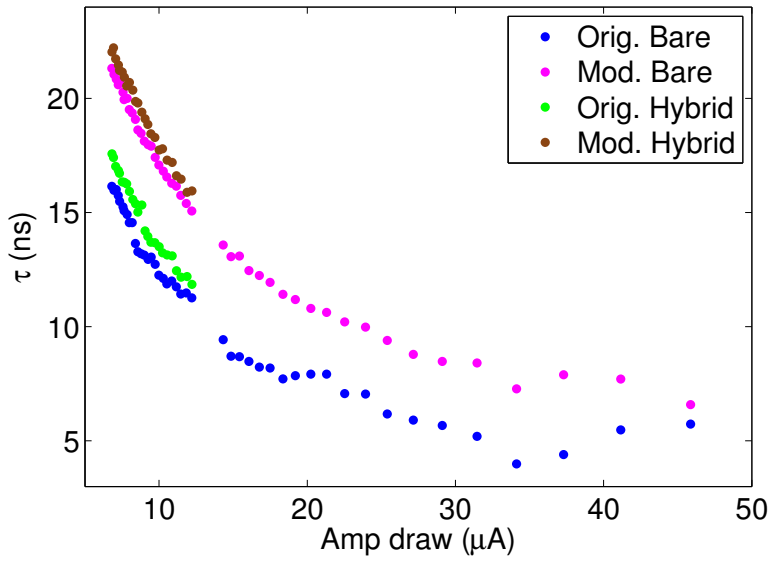
in Figure 6.1(b). The results of Figure 6.1(b) include the time for slew as well as the small-signal settling time.

The time constants and settling times found are slowed by the capacitive load of $\sim 170\,\text{fF}$ introduced by the injection capacitor. Recall the equations of section 3.2.1.2, particularly:

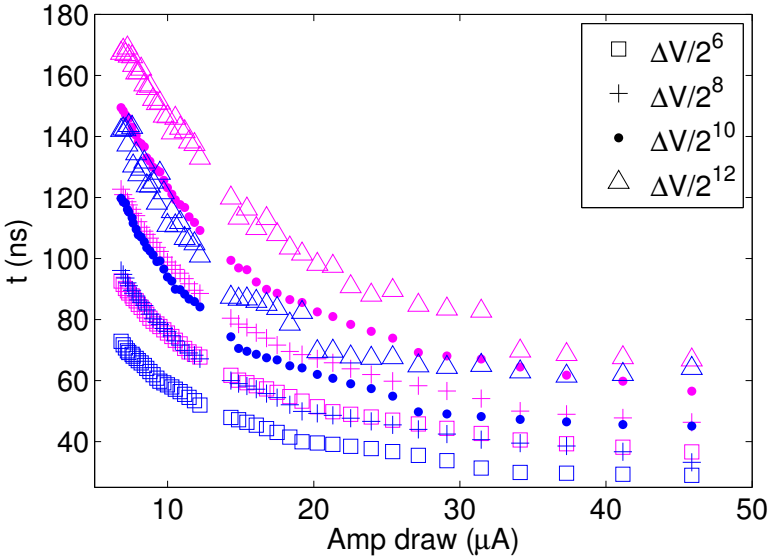
$$\tau = \frac{C_L C_F + C_L C_{IN} + C_{IN} C_F}{G_m C_F}. \tag{6.1}$$

Compared to an estimated detector layer and bump-bond capacitance of 75 fF the time constant of a pixel with the front-end capacitive load from the charge injector is estimated to increase by a factor of 1.34. At $10\,\mu\text{A}$ total draw a transconductance of $60\,\mu\text{S}$ and $40\,\mu\text{S}$ are extracted for the original and modified amplifier, respectively.

The amplifier was modified because of a slight overshoot in response to a charge impulse shown by the original amplifier. The overshoot is most pronounced when the feedback capacitance is large and, hence the feedback factor is near unity. Figure 6.2 shows the time for settling to levels of precision differentiated by the original and modified amplifier designs for $C_F = 1966\,\text{fF}$. Given the large feedback capacitance the voltage change induced was limited at 122 mV. For this experiment overshoot (around 2 mV) was seen at high amplifier bias currents and was most pronounced for the original amplifier. However, as seen in Figure 6.2 the original amplifier still reached values of settled precision as fast or faster than the modified amplifier. Slowing due to overshoot is evident by the upturn of the 10-bit resolution settling time at amplifier dissipation of $20\,\mu\text{A}$ or more. For this experiment, since the voltage change was low, results are only reported to a precision up to $\Delta V/2^{10} = 120\,\mu\text{V}$ (which is close to the noise floor of this experiment). For this feedback capacitor configuration one 8 keV x-ray produces a voltage change of $180\,\mu\text{V}$.



(a)



(b)

Figure 6.1: Small-signal time constant and time to reach levels of settled precision versus the current dissipated by the front-end amplifier measured by injection of a charge packet with C_F = 300 fF. (a) shows the time-constant versus the amplifier current draw. (b) shows settling to various levels of precision as indicated in the legend. This measure combines the time needed for slew and the small-signal settling. Results from the original pixel design are shown in blue and modified design in magenta. The precisions reached are ±12.4 mV, 3.1 mV, 772 μV, and 193 μV.

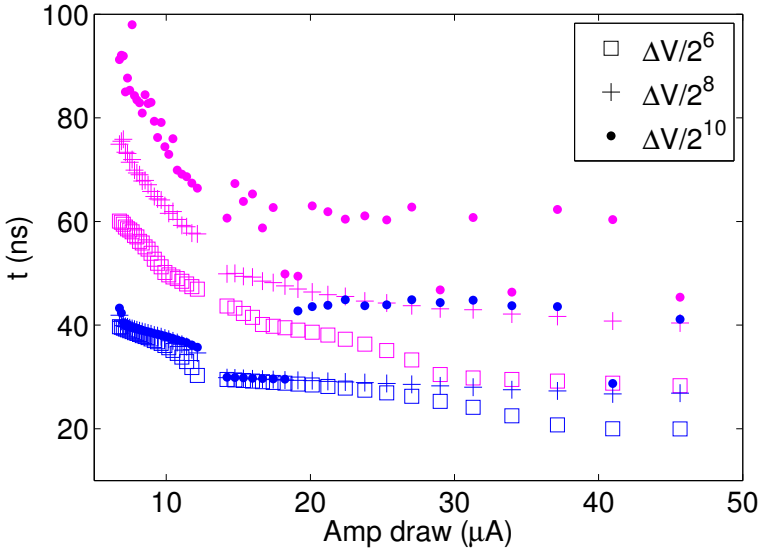


Figure 6.2: Settling to various levels of precision as indicated in the legend for $C_F = 1966\,\text{fF}$. Results from the original pixel design are shown in blue and modified design in magenta. The precisions reached are $\pm 1.9\,\text{mV}$, $477\,\mu\text{V}$, and $120\,\mu\text{V}$.

6.1.2 Maximum possible settling speed

The minimum possible settling time of the ASIC was explored for application to the Cornell Electron Storage Ring (CESR) test accelerator studies, bunches separated by 14 ns. Of course, the $500\,\mu\text{m}$ thick silicon detector layer limits the fastest collection time to 8.3 ns for velocity saturated hole collection ($\sim 900\,\text{V}$ bias). A thinner detector layer would be necessary if the ASIC is used for CESR test-accelerator.

Experiments first explored the maximum current draw of the front-end amplifier. The fastest response to injected charge was found with an external resistance, $R_{EXT} = 6.2\,\text{k}\Omega$, from the supply to the current mirror gate. This configuration resulted in a total chip supply draw of 72 mA which gives an estimated current draw of $240\,\mu\text{A}$ by the front-end amplifier. At an even lower R_{EXT} values the chip current draw saturated at 88 mA.

Measurement of a settling speed of 14 ns was difficult with the charge injec-

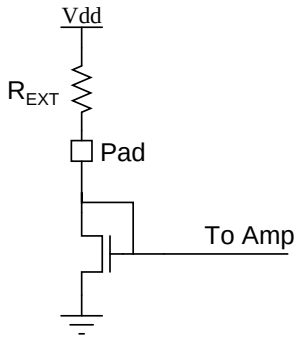


Figure 6.3: Schematic to show external resistance that determines amplifier bias. R_{EXT} is on the support printed circuit board.

tor because of the FPGA timing resolution of 10 ns and because the charge is injected by a capacitor through the resistance of a transistor switch which slows the injected signal. Experiments with C_F = 1966 fF found incomplete settling 10 ns after injected charge but complete (low accuracy) settling after 20 ns for injected charge of 50 fC to 235 fC (output voltage change from 0.025 to 0.12 V). The smaller injected charge packets were not settled significantly faster, probably because the AB action of the amplifier was not activated.

Transient simulations were also performed to avoid the time-step resolution set by the FPGA control electronics and to estimate the slowing inherent to the charge injection circuit. Transient simulations showed 7-8 ns was required for settling a charge impulse of 27 fC to 270 fC from a pulsed current source. Simulations with equal amounts of charge injected by the charge injector circuit generally slowed the response by only a few nanoseconds. Again, it was found that smaller injected charge packets did not settle significantly faster because the amplifier slew rate was less with a smaller input.

Isolation of successive bunches requires time to settle the signal and time to reset the amplifier, therefore, segregation of the 14 ns spaced bunches for CESR test accelerator studies seems tenuous. To do so with more confidence in a future ASIC fabrication, transistors would need to be resized to allow for higher

maximum current at lower overdrive voltages.

6.1.3 Selection of modified versus original pixel components

The larger transconductance of the original front-end amplifier versus the modified amplifier resulted in faster response despite a slight overshoot. Future submissions could use either amplifier but the original design was found to settle faster. A further redesign that maintains the amplifier transconductance but extends the phase margin would improve the settling time[1]. The front-end amplifier should be simulated along process corners to ensure that the stability is sufficient independent of fabrication variations.

The original ASIC half also showed higher read-noise values than the modified half. The noise increase is hypothesized to be due to the different pixel output buffer and storage capacitor switch configuration. Selection among the three modified and original design approaches (see section 4.2.1) advised for future fabrications with motivation in parentheses are as follows: original front-end amplifier (faster), modified storage capacitor switch configuration (less cross-talk, less noise), and modified in-pixel output buffer (most critical–significantly more radiation hard).

6.1.4 Support electronics development

PAD functionality and flexibility is set by the off-chip FPGA control as much as it is by the readout ASIC. Further developments to the FPGA control code would facilitate a broader range of experiments. Possible projects include FPGA

[1]The relationship between the fastest phase margin for settling-time to a desired accuracy is complex. In sampled data systems the flatness of frequency response is of no concern such that, if low levels of settled accuracy are required, an underdamped response settles faster than a critically damped response [136].

code for free-running acquisition that is halted by an external trigger signal. This feature would be most beneficial for experiments with non-repetitive sample dynamics that conclude faster than a trigger signal could be detected and sent to the PAD. Another example is to configure the FPGA to allow for external triggering of the transitions between accumulation elements.

6.1.5 Front-end noise considerations

The pixel front-end amplifier was designed with a primary goal of maximum settling speed with minimal static power dissipation, which motivated the use of a class AB amplifier. Minimization of the amplifier thermal noise was not a high priority. Partially, this was because previous experience had shown off-chip digitization circuits to set the detector noise above the noise of the PAD pixel. However, the off-chip electronics did not limit the noise of the small-area camera rather, the noise floor was set by the pixel. A simpler design with fewer transistors contributing could reduce the front-end amplifier noise. A single-ended amplifier would be a lower noise approach than a differential amplifier but is anticipated to be hindered by a lack of independent control of the pixel electrode voltage, robustness to radiation induced transistor threshold shifts, and instability in high-flux environments [48, 95]. These assertions of the limitations of a single-ended front-end amplifier should be experimentally tested with a fabricated design.

Further experiments could separate the noise contributions with standard Φ_{OR} operation shown in Table 5.1 into sampling of the front-end amplifier and configuration of the output buffer with capacitive feedback. One technique to do so would be to digitize a single pixel read multiple times to reduce the noise from the in-pixel output buffer. Since the front-end noise is sampled multi-

ple reads will not reduce this noise, whereas multiple reads would reduce the noise contribution from the output buffers. This measurement would determine whether the larger noise measured on the original ASIC half was due to the differences in the front-end amplifier or the output-buffer and storage capacitor switch configuration. Reduction of pixel noise should be guided by the expected output digitization rate and resolution. For example, for 12-bit conversion over a range of 2.5 V the pixel noise of the small area camera is at the step-size of the least-significant-bit of the converter such that reduction of the pixel noise would provide limited improvement.

6.2 PAD development for the ERL

The Energy Recovery Linac (ERL) is a next generation x-ray source proposed for Cornell University. ERL plans call for a fundamental RF frequency of 1.3 GHz so that x-ray pulses will arrive at the experimental hutch at intervals of 770 ps [137]. Here, I propose a possible detector design to isolate single bunches at the ERL.

At the saturated velocity for holes in silicon of 6×10^6 cm/s a 600 ps collection time limits the detector thickness to, at most, 36 μm (with a bias of $\sim$ 1000 V). Bump-bonding of a monolithic detector chip of such a thickness to a readout ASIC would be mechanically difficult. A photodiode that approaches such a thickness could be developed in the CMOS of the readout chip. Incorporation of the photodiode within the readout ASIC adds considerable ease to the development of the detector. Photodetectors with rates that approach and exceed 40 Gbits/s have been developed for optical communications [138]. Long-haul communication with fiber-optics uses wavelength ranges of 1260 nm to 1565 nm–in this range silicon is entirely transparent and cannot be used as a photodetector. Photodetectors composed of germanium and III-V materials,

such as GaAs and InGaAs, are relied upon. However, short-haul communication (on-chip or board-to-board) is expected to operate at 850 nm since low-cost vertical-cavity surface-emitting lasers are available at this wavelength. This has motivated significant work on the development of fast silicon photodetectors in standard CMOS since, at 850 nm, silicon is an effective detector. The absorption length of silicon at 850 nm wavelength is 16.5 μm, so that developments have maximized the thickness of the photodetector for detection efficiency to thicknesses that are compatible with low-energy x-ray detection.

Reference [139] has developed integrated silicon PiN diodes in standard 0.18 μm CMOS with FWHM pulse response of 127 ps. The photodetector design was carefully considered for a thick fully-depleted collection volume and to prevent slow collection from the un-depleted depths of the substrate. The work presents a deep N-well based photodiode shown to have bandwidths of 2.2, 3.2, and 4.0 GHz at bias voltages of 5, 10, and 15 V, respectively. The pulse response and bandwidths are sufficiently fast to keep pace with the repetition rate of the ERL x-ray pulses. The photodetector covered an area of $70 \times 70\,\mu m^2$ with interdigitated fingers to reduce the charge transit times. The efficiency at 5 V bias was measured as 21%, part of which was reduced due to the lack of an antireflection coating and the metal contacts on the photodiode fingers (both of these effects would not reduce efficiency with x-rays). Simulations predicted an efficiency of 30% from which a collection depth of 5.8 μm can be calculated. Of course, the efficiencies for x-ray stopping with this thickness of silicon are far from unity but not untenable (see Figure 6.4). Since this photodiode was incorporated into a standard CMOS process development of a two-dimensional imaging array should be feasible. Possible readout ASIC circuits are discussed below.

Another approach for high-speed and efficient detection is to change the geometry so that the thickness that sets the efficiency is not coupled to the carrier collection time or photodiode capacitance. This is the approach taken by certain germanium detectors for efficient IR detection at 1550 nm and 42 GHz bandwidths [140]. The geometry in Reference [140] is a detector 15 μm long and 3 μm wide. The electrodes were on both sides of the width of the device so that the collection times were set by the 3 μm width. The incident radiation propagates parallel to the length so that the efficiency was set by the 15 μm length. It is not clear how this approach could be configured into a two-dimensional pixel array, however, a one-dimensional array could be possible.

The work in [141] changed the geometry of standard planar x-ray detector layers by deposition of electrodes that penetrated the detector bulk (3D detectors). The electrodes were spaced 25 μm apart and the detector thickness was 300 μm. Charge is collected in the dimension perpendicular to the detector thickness so that the time for collection is set by the electrode spacing. Simulations showed a collection time of ~ 1 ns [141], yet, to the best of my knowledge, this has not been shown experimentally.

Other photodetectors with greater densities than silicon would more efficiently stop x-rays at an equal thickness. The literature must be carefully filtered; some high density photodetector developments, for example, InSb, are developed exclusively because the low bandgap energy of these materials renders sensitivity at deep IR wavelengths. However, the low bandgap of these detectors makes the thermally generated dark current significantly large to often require liquid nitrogen cooling.

GaAs is a detector material with a density considerably higher than silicon (5.3 versus 2.3 g/cm^3), a bandgap amenable to room temperature oper-

ation (E_g = 1.4 eV), and carrier mobilities of 8000 cm^2/Vs for electrons and 400 cm^2/Vs for holes [33]. GaAs detector arrays of 32×32 pixels and 325 μm thickness have been developed with almost Fano limited x-ray spectrum acquired at 5.9 keV [142].

Velocity saturated limited collection times of electrons in silicon and GaAs are 200 ps for thicknesses of 20 μm and 24 μm, respectively. The x-ray stopping efficiencies for silicon and GaAs versus thickness is shown in Figure 6.4 for multiple x-ray energies. Chips have been thinned to thicknesses of 150 μm before bump-bonding [143] so engineering hurdles certainly exist for hybridization of a ~20 μm thick detector layer.

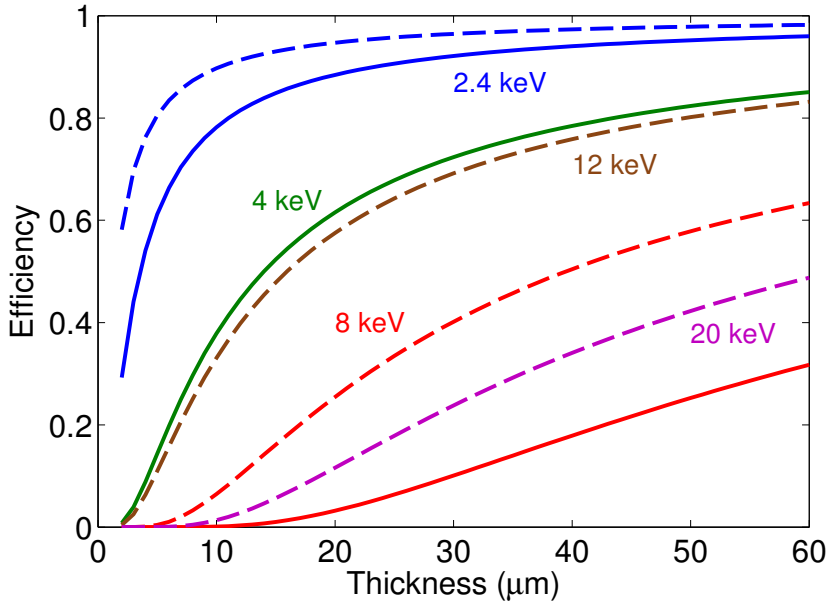


Figure 6.4: X-ray detection efficiency for Si (solid) and GaAs (dashed) at thicknesses less than 60 μm. Colors indicate energy of normally incident x-rays. GaAs has absorption edges at 10.4 keV and 11.9 keV.

Below is a non-exhaustive list of three paradigms possible for the readout circuit:

1. Source-follower buffer [53].
2. Integration capacitor with switch isolation (direct injection) [144].

3. Capacitive transimpedance amplifier (the approach of this dissertation) [145, 53].

The first two approaches are most appropriate for pixel arrays with isolated photodiodes. This is because the pixel electrode is not held at a constant voltage as charge is integrated. The DC charge-to-voltage gain for 1 and 2 depends upon the photodiode capacitance. The gain of the amplifier in approach 3 maintains the pixel electrode at a constant voltage which is particularly beneficial to limit pixel to pixel cross-talk through a common detector layer.

Appealing to equation 6.1 with a load capacitance, $C_L = 100\,\text{fF}$, a detector capacitance, $C_{IN} = 50\,\text{fF}$, and a feedback capacitance, $C_F = 200\,\text{fF}$ a transconductance of $875\,\mu\text{A/V}$ is required for a 200 ps time constant. This transconductance is possible with an NMOS transistor in $0.25\,\mu\text{m}$ CMOS with $100\,\mu\text{A}$ drain current. With thin detector layers biased at fields sufficient for velocity saturation and readout transistors biased with high drain currents an imaging device to isolate successive pulses from the ERL could be developed. New approaches for sampling clock distribution would be necessary. Possible approaches are on-chip PLL-based clock multiplication [52] or on-chip delay elements [144].

6.3 Conclusions

The 16×16 pixel device is not just a prototype for a larger area detector. As is, the camera is a unique device that offers many characteristics that far improve upon those of other x-ray detectors currently used for single bunch experiments. Table 6.1 compares a few important characteristics of devices that have been shown to isolate single synchrotron bunches. The devices include an "analog" avalanche photodiode (APD) that has the output amplified and then digitized by an oscilloscope, the Pilatus photon counting PAD configured to isolate single

bunches by gating the in-pixel counter, a photon counting APD, and the analog PAD presented in this work.

Table 6.1: Comparison of single-bunch resolving x-ray detectors for an experiment that detects a 2×2 mm^2 diffraction spot. ph/pix is the maximum number of photons detected per pixel per bunch. ph/spot is the maximum number of photons detected in a 2×2 mm^2 spot per bunch.

Device	Area (mm^2); pixels	ph/pix	ph/spot	Read time
Analog APD [56]	5×5; 1	500	500	N/A
Gated Pilatus 100K [18]	83.8×33.5; 487×195	1	144	2.7 ms
Counting APD [146]	5×5; 1	1	1	N/A
16×16 PAD (this work)	2.4×2.4; 16×16	2,000	3×10^5	600 μs

Consider the signal to noise possible for an experiment that detects a 2×2 mm^2 diffraction spot. In a single shot the detector in this work could make a measurement with a Poisson limited accuracy of 0.2%. The analog APD would be limited to 4.4% accuracy and the gated Pilatus PAD limited to 8.3%. The much greater single-shot Poisson limited accuracy of the device in this work would particularly facilitate experiments on fast single-shot or random events. The pixelated devices (Pilatus and this work) may detect angular motions in the diffraction spot in addition to the intensity. Another advantage inherent to the analog PAD presented here is the in-pixel storage which allows for isolated recording of eight consecutive bunches; the Pilatus detector is not capable of making such a measurement. In a pump-probe experiment the probe laser is typically pulsed at a rate of 1 kHz [14] which is slower than the readout rate of the 16 × 16 camera. An experiment using a photon counting APD must record for 5 s and probe the sample with 5,000 laser pulses to match the number of pho-

tons that could be detected in a singe shot with the analog PAD. Single Bragg spot time-resolved studies, especially of non-repetitive sample dynamics, are an excellent experimental match for the detector described.

APPENDIX A

POINTERS TO COMPUTER FILES

The list below points to computer files for schematics, layouts, computer code, and mechanical drawings that were created for this thesis work. It is my opinion that pointers to the actual computer files are more useful than, for example, a schematic presented here as a figure. Schematics were generally divided into a clean version meant to match the layout for layout-versus-schematic verification and into a scratch version for simulations. PCB folders generally contained folders titled 'ManufacturerFiles' which are the Gerber files submitted to the Fab-House, a folder titled 'BOM' with information on the bill-of-materials for population of the board, and a folder 'Datasheets' that includes the data-sheets for selected components used on the board.

The software used was as follows:

- IC Layouts: Tanner L-Edit (~v12.5)
- IC Schematics: Tanner S-Edit
- PCB design: EAGLE (4.16) from Cadsoft. Schematic extension: .sch, board extension: .brd
- FPGA design: Xilinx ISE (v9.1)
- Enclosure: Google sketchup

File pointers:

- **TB1**⇒ Amplifier test-bench:
  KECK_APSPAD\TestBench_forDistribution\TestBench\
- **SchP1**⇒ Schematic for prototype 1:
  KECK_APSPAD\Submission_1_Clean\LayoutSchematic_KECK_Mosis1\...
  LayoutSchematic_KECK_Mosis1.tanner
- **LP1**⇒ Layout for prototype 1:
  KECK_APSPAD\Submission_1_Clean\Layout\Layout_23June08.tdb
  Notes: Submission date: Sept-05-2008; TSMC-0.25-micron, SCN5M_DEEP, lambda=0.12 μm; FabID: T89RAB; 30 chips packaged in PGA108M, 10 chips left bare; GDS submission file: Top.gds
  Bonding diagram: KECK_APSPAD\Submission_1_Clean\...
  LayoutSchematic_KECK_Mosis1\PostSubmission_Documents\
- **SimP1**⇒ Simulations for prototype 1:
  KECK_APSPAD\Submission_1\Simulations\
  simulation schematic:
  KECK_APSPAD\Submission_1_Submission_1.tanner
- **PcbP1**⇒ Printed circuit board for prototype 1:
  KECK_APSPAD\Submission1_ReadoutControl\PCB_v1\
- **SchP2**⇒ Schematic for prototype 2:
  KECK_APSPAD\Submission_2_Clean\LayoutSchematic_KECK_Mosis2\...
  LayoutSchematic_KECK_Mosis2.tanner\
- **SimP2**⇒ Simulations for prototype 2:
  KECK_APSPAD\Submission_2\SEditForSims

- **LP2**⇒ Layout for prototype 2:

  KECK_APSPAD\Submission_2_Clean\Layout\KECK_MOSIS2.tdb

  Notes: Submission date: Apr-20-2009; TSMC-0.25-micron, SCN5M_DEEP,

  lambda=0.12 μm; FabID: T94C-AA; GDS submission file: Top.gds;

  10 chips packaged in PGA108M, 30 chips left bare;

  7 hybrids received from Polymer Assembly Technology

  (James Clayton: jclayton@polymerassemblytech.com)

  Bonding diagram:

  KECK_APSPAD\Submission_2_Clean\Bonding_Diagram_MOSIS\

- **CSP2**⇒ Control software for prototype 2:

  KECK_TESTER2\workspace\SPI_pydev_API\src\CamCtrl.py

  Experiment scripts:

  KECK_TESTER2\workspace\SPI_pydev_API\CamCtrlScript\

- **FpgaP2**⇒ FPGA code:

  KECK_APSPAD\Submission2_ReadoutControl\OpalKelly_ISEproj\...

  CameraCtrl\CameraCtrl.ise

- **PcbP2**⇒ PCB for prototype 2:

  KECK_APSPAD\Submission2_ReadoutControl\PCB_v0_proj\...

  KECK_Proto2_PCB_v0\

  PCB schematics in .pdf, .ps format:

  KECK_APSPAD\Submission2_ReadoutControl\PCB_v0_proj\...

  PCB_documentation\

- **EncP2**⇒ Enclosure for prototype 2:

  KECK_APSPAD\Submission2_ReadoutControl\Enclosure\...

  KECK_p2_Enclosure_v3.skp

  pdf Drawings: KECK_APSPAD\KECK_ReadoutControl\Enclosure\

APPENDIX B

16×16 CAMERA DATA AND CONTROL CODE ORGANIZATION

Data acquired with the 16×16 camera is organized by the date acquired in:
KECK_TESTER2\KECK_APSPAD\Submission2_ReadoutControl\TestData\
Control scripts to acquire data are organized by date and found in:
KECK_TESTER2\KECK_TESTER2\workspace\SPI_pydev_API\CamCtrlScript
Codes for analysis are organized by date and are found in the directory:
KECK_APSPAD\Submission_2_DataAnalysis\Matlab_Image_Analysis

APPENDIX C

16×16 OFF-CHIP BIAS CONTROL

The text header files that accompany the data files are a source of information for nominal operating configurations. The headers contain the setting of the operating parameters discussed in Table 4.2. The bias settings are indicated as an integer from 1-255. For current mirrors the resistance set by the potentiometer is given by 100 kΩ*(bias_setting/255). For reference voltages the voltage is given as 3.3 V*(bias_setting/255).

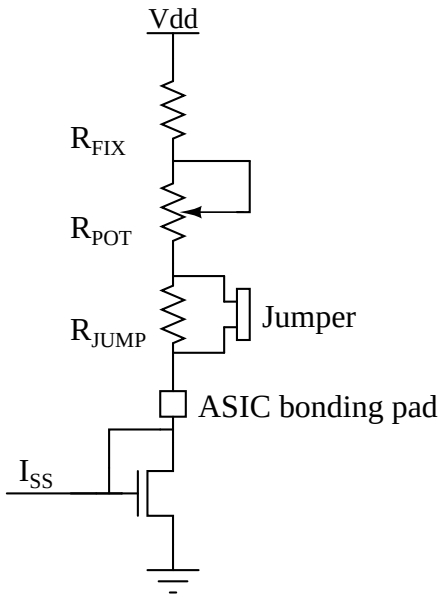


Figure C.1: Example, using an NMOS device, of the off-chip resistive network for current mirror biasing. R_{FIX} = 11 kΩ, R_{JUMP} = 110 kΩ, R_{POT} = 100 kΩ maximum (8-bit potentiometer step resolution). Standard operation bypasses R_{JUMP} for all amplifiers except the class AB front-end. For front-end dissipation ammenable to larger arrays R_{JUMP} is not bypassed for the AB amplifier. For high power 16 × 16 device operation R_{JUMP} may be bypassed.

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