An Accumulating Pixel Array Detector for Single-Bunch Synchrotron Experiments

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***Abstract*—We describe the development of a CMOS read-out chip for an x-ray pixel array detector that accumulates into analog storage elements with time resolution typical of synchrotron bunch spacings. Each pixel contains multiple analog storage elements to allow capture of full-frame images at submicrosecond separation. Additionally, each storage element is re-addressable, which allows accumulation of signal from temporally distinct acquisition windows. Test results show the ability to slew and settle the equivalent of 650 8-keV x-rays (1.21 Me^-) in less than 100 ns. The detector RMS read-noise was measured to be 2350 e^- and grows with the square-root of the number of accumulations with a coefficient of 415 e^- (equivalent to 1.07 and 0.19 8-keV x-rays respectively). The saturation value for each storage element, in terms of 8 keV x-rays, was measured to exceed 1880 x-rays (6.42 Me^-). The complete detector is anticipated to contain around 400 $\times$ 200 pixels with pixel size near 150 μm $\times$ 150 μm. Possible experimental applications include study of material failures, transient phase transformations, and high-speed x-radiography.**

***Index Terms*—CMOS analog integrated circuits, switched capacitor circuits, X-ray detectors, X-ray image sensors.**

I. Introduction

TWO-LAYER hybrid pixel array detectors (PADs) that leverage the flexibility of CMOS electronics have advanced synchrotron science in areas such as high-speed radiography of fuel-sprays, microsecond imaging of transient phase transformations, and x-ray microscopy [1]–[3]. PADs consist of a segmented high-resistivity detector layer bump-bonded to a pixellated read-out chip designed in standard CMOS technology. The approach for PAD read-out pixel electronics may be divided into two broad classes: those that digitally count individual photons (digital PADs) and those that integrate photo-charge and digitize the signal following acquisition (analog PADs).

X-ray synchrotrons produce pulsed x-ray beams from electron or positron bunches. The interbunch spacing sets the time between pulses and the bunch length sets the duration of the pulse (Table I). Digital PADs have low intrinsic noise and the timing resolution sufficient to isolate single bunches, but pixel-level shaping circuits process photon arrival at rates limited to 1–10 MHz. Since Poisson statistics limit the accuracy of a single measurement to $\sqrt{N}/N$ for the detection of N x-rays, a maximum of one x-ray counted per bunch per pixel of digital PADs constrains the achievable accuracy per bunch. Analog PADs have shown the capability to handle fluxes approaching 10^{12} x-rays/pixel/s and have approached, but not yet reached the timing resolution needed to isolate multiple single x-ray bunches in succession [4]. A detector capable of isolating the arrival of each x-ray bunch and acquiring hundreds or more x-rays per bunch would allow experiments with timing resolutions limited by the x-ray pulse width without optical pumping and complex x-ray choppers.

The detector pixel architecture described here captures signals on multiple analog storage elements in each pixel before readout. This allows each pixel to acquire multiple frames with sub-microsecond temporal resolution per readout. The pixels are also designed to allow re-addressing and addition of signal

TABLE I
Timing Parameters of Fill Patterns at Common Synchrotron X-Ray Sources and the Under-Construction European XFEL

Source	Bunch Spacing	Bunch Width
ALS [a]	2 ns	65 ps
ALS [b]	328 ns	65 ps
APS [c]	153 ns	20 ps
CHESS [d]	280 ns	5-bunch train
ESRF [e]	2.82 ns	20 ps (RMS)
ESRF [f]	176 ns	48 ps (RMS)
EXFEL [g]	200 ns	100 fs
NSLS [h]	18.9 ns	290 ps (2σ)
NSLS [i]	94.5 ns	290 ps (2σ)
NSLS [j]	567.2 ns	290 ps (2σ)
SLS [k]	1.88 ns	not found
SPring-8 [l]	23.6 ns	70 ps (FWHM)
SPring-8 [m]	145.5 ns	11 bunch train
SPring-8 [n]	342.1 ns	70 ps (FWHM)

[a] Advanced Light Source, Berkeley, CA, USA; multi-bunch mode.
[b] ALS: two-bunch mode.
[c] Advanced Photon Source, Argonne, IL, USA [19].
[d] Cornell High Energy Synchrotron Source, Ithaca, NY, USA.
[e] European Synchrotron Radiation Facility, Grenoble, France; standard operation.
[f] ESRF: 16-bunch mode.
[g] European XFEL at DESY, Hamburg, Germany [20].
[h] National Synchrotron Light Source, Upton, NY, USA; standard operation.
[i] NSLS: five bunch mode.
[j] NSLS: single bunch mode.
[k] Swiss Light Source, PSI, Switzerland.
[l] Super Photon Ring, Hyōgo Prefecture,Japan; 'A-mode': 203 bunches.
[m] SPring-8: 'C-mode': 11-bunch train $\times$ 29.
[n] SPring-8: 'D-mode': 1/14-filling + 12 bunches.

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to the storage elements following either the accumulation into a different storage element or electronic shuttering of the x-ray signal. A frame may thus be built from temporally separated acquisition windows. Each distinct window is referred to as an accumulation. Accumulation accomplishes in-pixel noise averaging before readout given a repeatable signal.

A potential application of the accumulation functionality is the study of a sample driven by an oscillatory stimulus. In this application, each storage frame would accumulate x-ray signal during different phases of the stimulus. A second possible application is the study of systems that produce distinct asynchronous triggers. The detector control system would be designed to link each frame to a unique trigger type. Following the detection and classification of a trigger, the detector would accumulate x-ray signal onto the appropriate frame element.

In this paper the concept of an analog accumulating PAD is presented, considerations regarding the pixel design are discussed, and calculations are shown to estimate the pixel performance parameters. Experimental results that include speed, linearity, noise, and radiation robustness are presented for a fabricated prototype Application Specific Integrated Circuit (ASIC).

II. Design

A. Specifications and Approach

The desired detector specifications in terms of 8 keV x-rays include:

1) Pixel size of $150\ \mu\mathrm{m} \times 150\ \mu\mathrm{m}$.
2) Array size of 400 $\times$ 200 pixels built from a 4 $\times$ 2 mosaic of three-side buttable CMOS chips.
3) ASIC radiation tolerance greater than 100 kGy(Si).
4) Power per pixel of $< 100\ \mu$W with a supply voltage of 3.3 V.
5) Minimum integration time of 150 ns or less given an incident signal of up to 1000 x-rays/pixel/150 ns.
6) At least 100 separate accumulations into each storage element possible before readout.
7) Noise less than 0.5 x-rays/pixel/accumulation and a readout noise less than 1.0 x-rays/pixel.
8) Five or more storage elements per pixel with a capacity exceeding 2000 x-rays each.

Two paradigms explored for an accumulating charge integrating readout ASIC are shown in Figs. 1 and 2. Both of these pixel architectures, in the form of test structures but not of a final pixel entirely appropriate for use within a hybridized detector, have been fabricated and tested. The first approach uses a switched-capacitor storage stage (shown in Fig. 1) at the pixel back-end. After closing all switches to clear charge across capacitors, the pixel timing for accumulating onto storage element C_{S1} proceeds as follows:

- All Φ_S opened, Φ_F, Φ_R closed.
- Φ_F opens.
- Φ_R opens sampling the reset of the front-end and beginning integration. Soon thereafter Φ_{S1} closes.
- Exposure time: integrate charge Q.
- Φ_{S1} opens ending the integration and leaving a voltage: $V_{REF2} + (Q/C_F)(C_1/C_{S1})$ at $\mathrm{PIX_{OUT}}$.

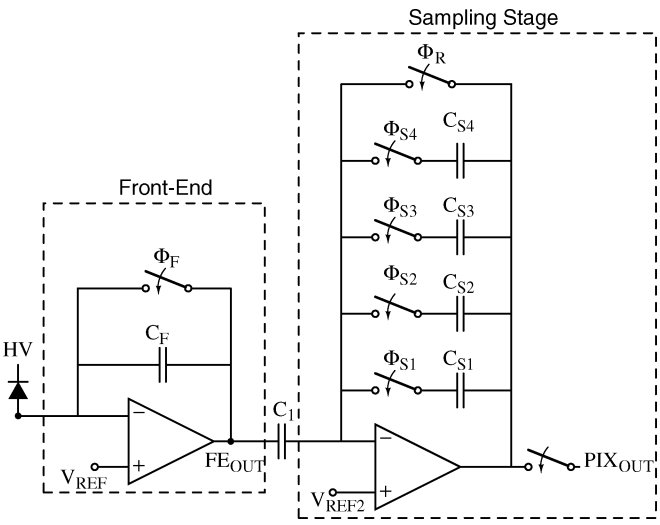

Fig. 1. A simplified schematic of the pixel that uses a switched-capacitor discrete-time integrator to accomplish accumulation in the pixel.

The second approach uses the front-end integration capacitor as the storage element during accumulation (shown in Fig. 2). Accumulation is accomplished via switches Φ_{F1-4}. At the end of each frame the front-end output is captured by one of an array of capacitive storage elements (C_{S1-4}) for later readout. During readout switch Φ_{SE} is opened to disconnect the front-end from the sampling stage. Then Φ_{BP} is opened, Φ_{RE} closed, and switches Φ_{S1-4} are used to connect the correct storage capacitor across the readout amplifier to buffer the stored voltage onto the readout bus. The sampling stage captures successive frames with or without the use of accumulation at the front-end. Two-bit front-end charge-to-voltage gain selection is possible when accumulation is not used. A final version of the detector would include more storage capacitors to increase the number of distinct temporal snap-shots when accumulation is not utilized.

The approach of Fig. 1 with accumulation at the back-end of the pixel requires slewing and settling of two amplifiers during each sampling period, but decouples the charge-to-voltage gain and full-well of the pixel from the thermal noise added to the signal during each accumulation. The approach with accumulation at the front-end (Fig. 2) requires the slewing and settling of only one amplifier during each sampling period but the charge-to-voltage gain and full-well of the pixel are linked to the thermal noise during each accumulation. Experiments described and discussed later in Section III will determine which pixel architecture is most appropriate for the desired detector characteristics.

Slewing, small-signal settling time, noise, and saturation value may be considered with reference to the schematic shown in Fig. 3 with assumptions of $C_F = 400$ fF, $C_L = 400$ fF, and $C_{IN} = 130$ fF. For example, an integration capacitor $(\mathrm{C_F})$ of 500 fF gives a full-well of 2140 8-keV x-rays with a front-end amplifier swing of 1.5 V $(\Delta V_{\mathrm{x-ray}} = 700\ \mu\mathrm{V})$. A full-well of 2140 x-rays allows for a Poisson limited accuracy of $\sqrt{2140}/2140 = 2.2\%$ per-pixel in a single frame. Noise considerations per accumulation require a large front-end load capacitance $(\mathrm{C_L})$ while speed and area considerations suggest a small capacitance. The input capacitance $(\mathrm{C_{IN}})$ is

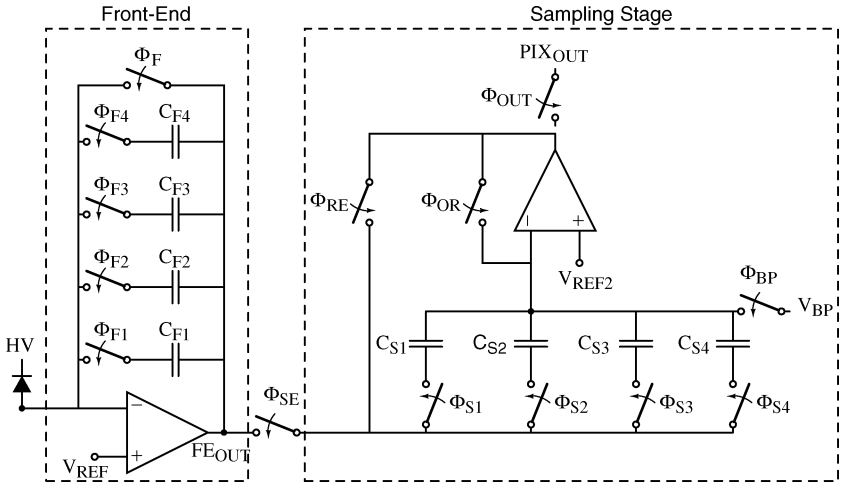

Fig. 2. A simplified schematic of the pixel that incorporates accumulation at the front-end integration capacitors.

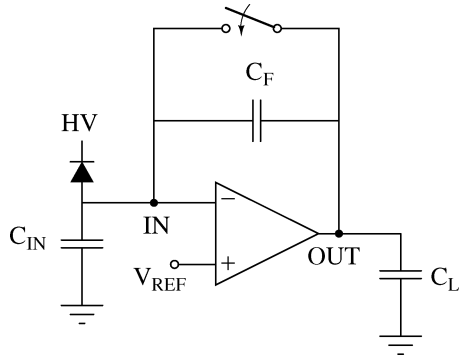

Fig. 3. Schematic of a PAD front-end for settling time and slewing considerations.

anticipated to include 60 fF due to the detector layer [5], 55 fF due to the amplifier input devices and 15 fF due to the input bump-bonding pad, totaling 130 fF.

B. Settling Time and Slew Rate

For a properly compensated single-stage amplifier, with transconductance, g_m, and DC-gain, A_0, configured as in Fig. 3, the small-signal settling-time is given as $\tau = C_O/(\beta g_m)$, with $C_O = C_L + (C_{IN}C_F/(C_{IN} + C_F))$, the feedback factor, $\beta = C_F/(C_F + C_{IN})$, and $A_0 \gg \beta$ [6]. A maximum transconductance to current ratio of $g_m/I_D = 1/(n\phi_T) = 28.5\ \mathrm{V}^{-1}$, where ϕ_T is the thermal voltage and $n \approx 1.3$ is the reciprocal slope factor, is found when transistors are biased in deep weak inversion [7]. Simulations show for a differential folded cascode amplifier, an architecture chosen to support a large voltage differential between the input and output, $g_m/I_{tot} = 5\ \mathrm{V}^{-1}$ (each input device receives $I_{tot}/4$, where I_{tot} is the total current dissipated by the amplifier). Single-ended input amplifiers and single-branch amplifiers (for example a telescopic cascode) would have a larger g_m/I_{tot} value but are not explored due to poor power supply noise rejection and radiation robustness of single-ended input amplifiers and limited voltage swing of single-branch amplifiers. Settling to M-bit accuracy requires $t = \tau M \ln(2)$. Small-signal settling to 8-bit accuracy (8-bit accuracy, 0.4%, comfortably exceeds the Poisson limited accuracy of the full-well acquisition of 2000 x-rays, 2.2%) given the parameters in Fig. 3 and the transconductance to current ratio discussed above requires a time of,

$$t_{settle} = \frac{730}{I_{tot}}[\mathrm{ns} \cdot \mu\mathrm{A}]. \tag{1}$$

Next front-end slewing of large input signals is considered. For this discussion the detector layer is considered to provide a delta-function current impulse; in reality a current is seen at the p-type electrode with a duration given by the hole collection time. Given standard operating parameters of a 500 μm thick Si detection layer the hole collection time is constrained at less than 30 ns [8]; thus, charge collection will not limit time resolution in a way that prevents single-bunch imaging. Immediately after arrival of a charge impulse, Q_{IN}, the pixel is considered to contain only the three capacitors (C_F, C_L, C_{IN}), as the amplifier has a finite response time. The voltage at the front-end output increases by [5]:

$$\Delta V_{OUT} = Q_F \frac{C_F}{C_F C_L + C_F C_{IN} + C_L C_{IN}} \tag{2}$$

(an example of this voltage jump is displayed from 0–10 ns in Fig. 7(a)). The pixel input increases similarly and needs to be maintained below the level that forward biases the source-bulk junction of the PMOS Φ_F switch, otherwise signal charge is lost to the supply. The output voltage settles to $V_{REF} - (Q_{IN}/C_F)$ giving a voltage to slew of

$$V_{SLEW} = \Delta V_{OUT} + \frac{Q_{IN}}{C_F}. \tag{3}$$

The capacitance to slew is the addition of the load capacitance and the series combination of the feedback and input capacitances giving a slew-rate, SR, of

$$SR = \frac{I_{load}}{C_L + (C_F C_{IN})/(C_F + C_{IN})} \tag{4}$$

where I_{load} is the current the amplifier supplies to the load during a slewing event. Given the capacitive parameters above the time for slew is

$$t_{slew} = \frac{0.75 \cdot Q_{IN}}{I_{load}} \left[\frac{\mathrm{ns} \cdot \mu\mathrm{A}}{\mathrm{fC}}\right]. \quad (5)$$

Summing the time for small-signal settling, (1), and the time for slewing, (5), gives the total 8-bit settling time,

$$t_{total} = \frac{730}{I_{tot}}[\mathrm{ns} \cdot \mu\mathrm{A}] + \frac{1.5 \cdot Q_{IN}}{I_{load}} \left[\frac{\mathrm{ns} \cdot \mu\mathrm{A}}{\mathrm{fC}}\right], \quad (6)$$

where a class-A amplifier that supplies half of the quiescent current to the load during a slewing event has been assumed. If the current to the load during slewing is not limited by the static bias current the time for slewing may be reduced without a corresponding increase in static power consumption. For this reason, a class AB amplifier has been designed and tested that responds to slewing events with a current to the load greater than the quiescent current. A dynamic amplifier diverts current to heavily illuminated pixels, which is advantageous in cases when only a fraction of pixels see the maximum flux specification.

C. Noise

The accumulation functionality has been developed to allow weak signals to surpass the read-noise floor. Noise will increase with the square-root of the number of accumulations since each sampling operation acquires a sample of transistor thermal noise that is uncorrelated with other samples. Thus, N accumulations enhances the signal-to-noise by $N/\sqrt{N} = \sqrt{N}$. Sampled thermal noise in the front-end accumulating architecture is divided into three distinct operations:

1) Noise sampled at the input during pixel reset when Φ_{F} is opened.
2) Noise sampled upon conclusion of an accumulation when Φ_{Fj} is opened (where j is 1–4).
3) Noise sampled onto a storage capacitor C_{Sj} upon the end of the frame.

Noise per accumulation is similar for the back-end accumulating architecture shown in Fig. 1 but gives higher values due to an increased number of switching events.

D. Class AB Amplifier

PADs are often built from a mosaic of multiple CMOS ASICs. To increase the contiguous imaging area of the detector wire-bonds are typically confined to a single-side of the die (making a three-side buttable device) and dies are designed to fill the stepper reticle ($\sim 20\ \mathrm{mm} \times 20\ \mathrm{mm}$). To reduce leakage current from the detector layer analog PADs generally operate at temperatures around $-20^{\circ}\mathrm{C}$. These approaches place challenges upon power dissipation in addition to power and ground distribution within the CMOS readout ASIC. Our experience suggests a power limit of $100\ \mu\mathrm{W/pixel}$. As explained earlier, pixel settling time will be limited by amplifier slew-rate limitations; therefore, a class AB amplifier has been incorporated to enhance current provided to the load in a slewing situation without an increase in quiescent power consumption. The class AB amplifier, shown in Fig. 4, is based on work by Carvajal and colleagues [9], [10]. Transistor groups $\mathrm{M0_{FA}}, \mathrm{M1_{FA}}, \mathrm{M2_{FA}}$ and $\mathrm{M0_{FB}}, \mathrm{M1_{FB}}, \mathrm{M2_{FB}}$ form a flipped voltage follower that presents a low-impedance level-shifted version of the input voltage to the sources of the opposite input transistor (M1, M2) and acts as an adaptive bias. Since a copy of the opposite input voltage is applied to the source of the input devices the effective transconductance of the amplifier is $g_m = 2g_{m1} = 2g_{m2}$, where g_{m1} and g_{m2} are the transconductances of devices M1 and M2 respectively. The diode connection at the gates of M3 and M4 may be removed and the drains of M1/M3 and M2/M4 resistively coupled to a node that connects the gates of M3 and M4 for larger current gain. The output branch could be cascoded for larger gain but maximization of voltage swing was preferred for this prototype.

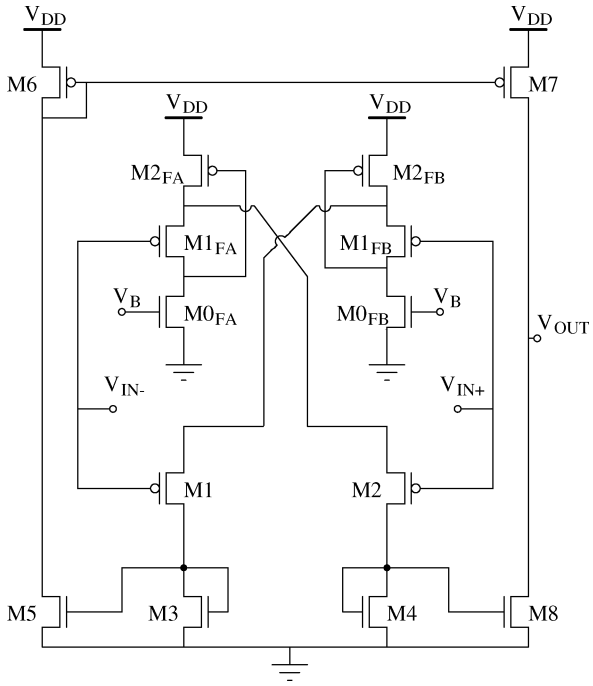

Fig. 4. Class AB amplifier schematic showing the active bias circuit based on the flipped-voltage follower (transistors $\mathrm{M0_{FA}}, \mathrm{M1_{FA}}, \mathrm{M2_{FA}}$ and $\mathrm{M0_{FB}}, \mathrm{M1_{FB}}, \mathrm{M2_{FB}}$) coupled to a standard current-mirror operational transconductance amplifier.

III. Experimental Results

A. Prototype ASIC

The prototype ASIC was fabricated through the MOSIS service in a TSMC mixed-mode, non-epitaxial substrate 0.25 $\mu\mathrm{m}$ CMOS process using thick-oxide 3.3 V transistors. The chip shown in Fig. 5 includes two individually addressable 6 × 8 pixel arrays. One of the 6 × 8 arrays contains pixels as shown in Fig. 1; the other array contains pixels as shown in Fig. 2. Pixels in this prototype measured around $100\ \mu\mathrm{m} \times 100\ \mu\mathrm{m}$. Each 6 × 8 (rows × columns) pixel array has an eight-to-one analog multiplexer that buffers the selected pixel output to a dedicated wire-bond pad. The analog multiplexers and row selection are controlled by two bit-passing shift registers. Further pixel monitoring is available through probe-pads at the front-end output

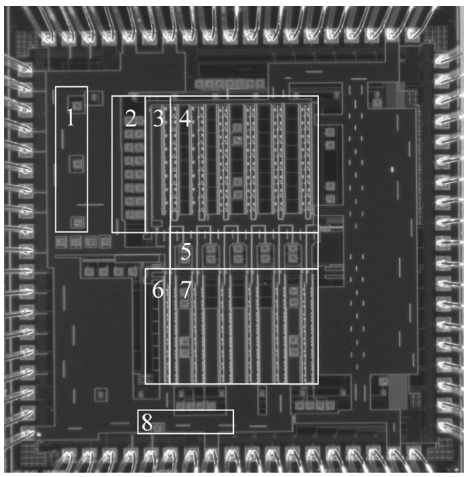

Fig. 5. A microphotograph of the prototype chip. The chip measures 3.3 mm × 3.3 mm. The labeled areas are as follows: 1) amplifier test structures, 2) column addressing register, 3) front-end accumulation array output multiplexer, 4) 6 × 8 front-end accumulation pixel array, 5) row addressing register, 6) back-end accumulation array output multiplexer, 7) 6 × 8 back-end accumulation array, 8) MOS transistor R-2R current-splitter.

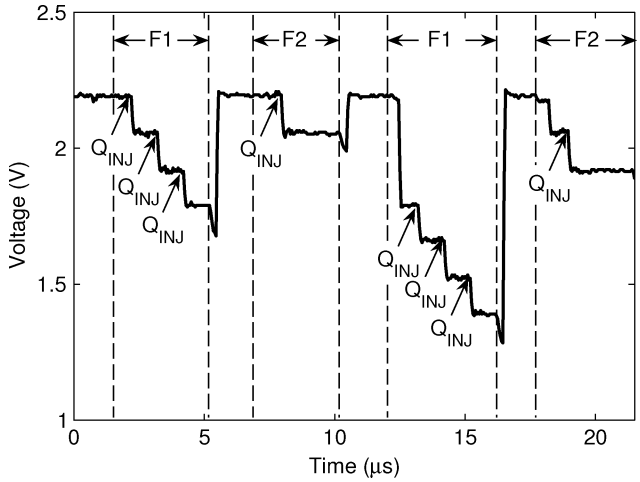

Fig. 6. Oscilloscope trace taken at node $\mathrm{FE_{OUT}}$ of Fig. 2 using a picoprobe that displays the accumulation function in the pixel. At each point indicated by Q_{INJ} a charge of 70 fC (equivalent to 200 8-keV x-rays) is injected into the front-end. The regions labeled 'F1' and 'F2' indicate respectively, acquisition onto the first frame element (C_{F1} in Fig. 2) and acquisition onto the second frame element (C_{F2} in Fig. 2). The second 'F1' and 'F2' regions begin at the voltage reached at the conclusion of the first region thus displaying the accumulation functionality.

$(\mathrm{FE_{OUT}})$ and the pixel output $(\mathrm{PIX_{OUT}})$ in four pixels per array. Three columns in each array have a 195 fF charge injection capacitor at the pixel inputs, three columns have a 6 fF charge injection capacitor, one column has a high-bandwidth p+/n+ photodiode [11], and one column has pixels without an explicit input source.

The test chip explores performance differences between two folded cascode amplifiers with a low-voltage cascode current mirror, one with NMOS input devices and a second with PMOS input devices, and the described class AB amplifier. Each amplifier design is used in two rows of both arrays. The chip also contains isolated amplifier test structures of all three types. Each amplifier test structure output is available at a wire-bond pad and a probe-pad. All NMOS transistors within the test chip are designed using radiation hardened layout techniques: Transistors with large width-to-length ratios are drawn using enclosed layout techniques [12] while transistors with smaller width-to-length ratios are drawn using a radiation hardened linear technique that dopes the edges of the polysilicon gate p-type to increase the threshold voltage of radiation-induced parasitic edge transistors [13]. Where a reduction in charge-injection is necessary to limit spurious signal during accumulation switches include a half-sized dummy switch driven by an inverted clock signal. Simple non-overlapping clock generators are used to control the switches in the sampling stage of Fig. 1 to minimize the time when the amplifier is configured without feedback. A radiation hardened version of the MOS transistor R-2R current-splitter, designed by Delbruck and van Schaik to digitally control bias currents and voltages on chip, was implemented as a test structure and confirmed functional [14]. For this prototype, arrays of storage capacitors were limited to four elements for simplicity and a reduction of wire-bond count. All experiments were performed with the chip in a light-tight enclosure and at room temperature.

B. Accumulation

Accumulation functionality was verified for both pixel varieties. The concept is illustrated in Fig. 6. The sequence of steps are delineated by dashed vertical lines and proceed as follows:

1) Pixel reset: any input signal is shuttered.
2) Accumulate three injection pulses onto frame 1 (F1).
3) Pixel reset: any input signal is shuttered.
4) Accumulate one injection pulse onto frame 2 (F2).
5) Pixel reset: any input signal is shuttered.
6) Re-address frame 1 (F1) and recover voltage stored at the conclusion of step 2 (at 5 μs). Accumulate three injection pulses onto frame 1. Frame 1 now holds the sum of the signal from step 2 and step 6 which equals six charge injection operations.
7) Pixel reset: any input signal is shuttered.
8) Re-address frame 2 (F2) and recover voltage stored at the conclusion of step 4 (at 10 μs). Accumulate one injection pulse onto frame 2. Frame 2 now holds the sum of the signal from step 4 and step 8 which equals two charge injection operations.

This architecture may also switch immediately between frames without intermediary shuttering of the x-ray signal.

An injected signal of 6 mV per accumulation was measured for the switched capacitor architecture due to charge injection and finite amplifier gain. Circuit non-idealities saturate the pixel in approximately 100 accumulation operations. Fully-differential sampling architectures would reduce spurious signal due to charge injection [15]; however the area and power costs need to be explored and may be prohibitive. The injected signal per accumulation was measured to be 500 μV for the front-end accumulation architecture. This architecture was found to reach an equilibrium where dark accumulations no longer inject spurious signal, thus allowing further accumulations without pixel saturation.

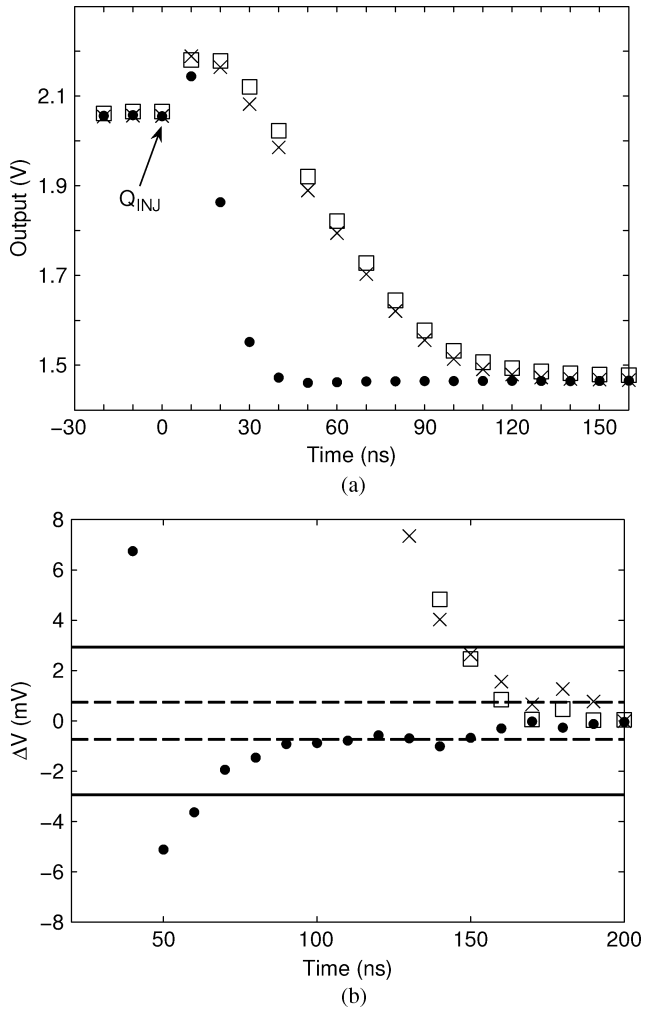

Fig. 7. (a) Comparison of front-end output slewing following injection of charge for the class AB amplifier (•), the NMOS input folded-cascode (×), and the PMOS input folded-cascode (□). (b) Small signal settling calculated from the data shown in (a). Plotted is the deviation (ΔV) from the final settled value versus delay time. The solid line indicates 8-bit accuracy given a 1.5 V range while the dotted line indicates 10-bit accuracy.

C. Settling Time

Pixel settling time was studied by varying the time between charge injection into the pixel input and the sampling of the front-end output by the storage stage. The value held by the pixel was then read out through the analog output chain. The output voltage measured is plotted versus the time between charge injection and sampling in Fig. 7(a). At $t = 0$ ns a charge of 240 fC (equivalent to 685 8-keV x-rays) was injected into the front-end. The size of the injection capacitor limited the total charge per injection. The results are shown for each amplifier configured at a static power consumption of 43 μW. Results were measured to be similar for the front-end accumulation architecture except for anticipated differences due to changes in loading capacitance. The class AB amplifier at a power dissipation of 43 μW slews the equivalent of 685 8-keV x-rays in less than 40 ns whereas the folded-cascode amplifiers require 100 ns. Fig. 7(b) shows the small-signal approach to the final value. The overshoot at 50 ns of the class AB amplifier reveals a deficient phase margin which will be adjusted in future fabrications. The slew-rate of the folded cascode amplifiers is calculated from (3) (with an adjustment for the loading of the injection capacitor) to be 11 V/μs whereas 8.8 V/μs is measured. The deviation is anticipated to be due to parasitic capacitance within the pixels. Another possible cause for the discrepancy is that the amplifiers supply less than half of the total bias current to the load during slewing (measured at ≈85% by simulation). Isolated class AB amplifier test structures configured in unity-gain and operated at 53 μW dissipation were found to drive larger load capacitances with a current of $I_{load} = 26I_{tot}$ and $I_{load} = 24I_{tot}$ for falling and rising slew operations respectively.

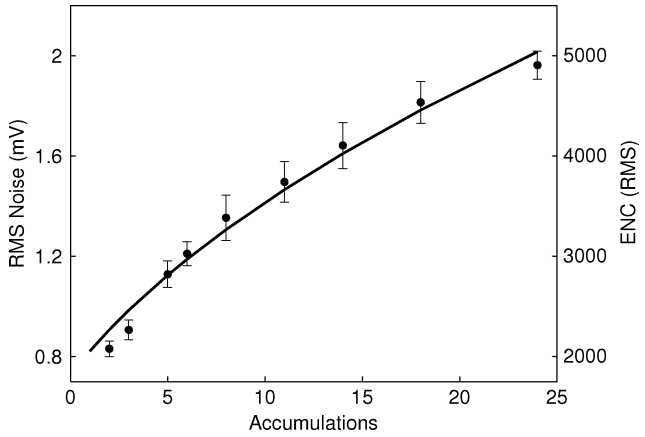

Fig. 8. Noise growth versus accumulations for the back-end accumulating pixel configuration using the class AB amplifier at both the front-end and the sampling-stage. A fit to the data using the model in the text is shown as a solid line. Error-bars represent the standard deviation of the noise measured between seven different pixels in the column.

D. Noise

The fixed read-noise and noise per accumulation was measured for both architectures and is shown in Figs. 8 and 9. The noise was found to have limited dependance upon amplifier architecture but was greatest for the class AB amplifier. A model of $\sigma^2 = A^2 + B^2 \times N$ was used to fit the data to estimate the fixed contribution from readout and pixel reset (A) and the contribution from each accumulation (B) with N the number of accumulations. A fit to the data shown in Fig. 8 for the back-end accumulating architecture return $A = 726\ \mu\text{V} = 1815\text{e}^-$ and $B = 384\ \mu\text{V} = 960\text{e}^-$. The noise dependence on the input capacitance was studied by placing an explicit load capacitor of 195 fF at the pixel input. Shown in Fig. 9 the noise per accumulation for the front-end accumulating architecture was measured to be $B = 183\ \mu\text{V} = 572\text{e}^-$ and $B = 132\ \mu\text{V} = 413\text{e}^-$ with and without an explicit capacitive input load respectively. The fixed contribution was measured to be $A = 729\ \mu\text{V} = 2278\text{e}^-$ and $A = 752\ \mu\text{V} = 2350\text{e}^-$ with and without an explicit capacitive input load respectively. A hybridized detector layer is anticipated to introduce a smaller capacitance, 130 fF, than the explicit test load, 195 fF. The noise power per accumulation was around twice as large for the back-end accumulation architecture as anticipated because of the larger number of sampling events per accumulation for this architecture.

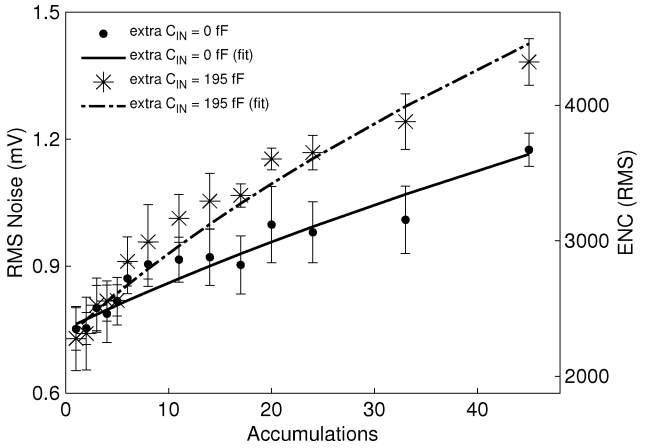

Fig. 9. Noise growth versus accumulations for the front-end accumulating architecture using the class AB amplifier at the front-end. Error-bars represent the standard deviation of the noise measured between eight different pixels without explicit capacitive load and six pixels with additional capacitive load.

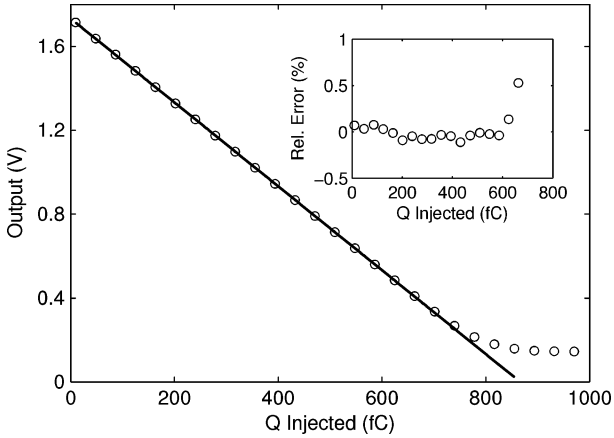

Fig. 10. Pixel output ($\circ$) and a linear fit (solid-line) plotted versus charge injected. The inset shows the Relative Error $(\mathrm{Rel.\ Error}(\%) = 100 \times (\mathrm{measured} - \mathrm{fit})/\mathrm{fit})$ for injected charge of up to 660 fC.

E. Storage Element Hold Times

Storage element hold times were evaluated using the front-end accumulation architecture. The charge injection circuit was used to vary the charge stored across C_{F1}. After injecting charge, switch Φ_{F1} was opened, the pixel front-end reset to V_{REF}, and the charge across C_{F1} was held for up to 12 s. After the specified hold time, the pixel value was readout. During a hold operation, with the pixel reset to V_{REF}, the Φ_{F1} switch source voltage, V_S, is given as $V_S = V_{REF} + (Q_{IN}/C_{F1})$. Forward biasing of the transistor source-to-bulk p-n junction limits the maximum V_S to V_{DD}. This limit suggests an optimal V_{REF} of $V_{DD}/2$ to maximize front-end swing without loss of signal through forward biased p-n junctions of switches Φ_{F1-4}. At levels of low injected charge the hold-switch gate-source voltage, V_{GS}, remains below -400 mV, so that the transistor is in accumulation-mode and subthreshold drain-to-source leakage current is minimal [16]. Leakage of 2 fA that increased the charge stored across C_{F1} was measured. When V_{GS} exceeds -200 mV the transistor enters weak inversion and drain-to-source current increases. The maximum leakage current measured was 0.5 fA discharging C_{F1} with $V_{GS} = -80$ mV and $V_{DS} = -1.57$ V. These results suggest that maximum exposure times are limited to seconds by the holding ability of analog storage elements. Further improvement of storage element hold times may not be fruitful as detector layer leakage ($\sim$100 fA/pixel) will limit the minimum resolvable x-ray flux. The above measurements were taken with the chip at room temperature. A reduction of leakage currents that corrupt storage elements is anticipated when the detector is cooled.

F. Linearity and Cross-Talk

Linearity and analog storage element cross-talk were evaluated by independently varying the number of charge packets of magnitude 9.6 fC injected into the front-end before storage onto C_{S1} and C_{S2}. Following injection both storage elements were read through the analog output chain. The pixel output for C_{S2} along with a linear fit is plotted versus the total charge injected in Fig. 10. The relative error of measured data from fit is plotted in the inset and remains below 6×10^{-3} for injected charge up to 660 fC (equivalent to 1880 8-keV x-rays). For this experiment only one C_F capacitor was connected across the front-end amplifier. For flash-mode operation or accumulation onto only a single frame the full-well could be increased fourfold by engaging all C_{F1-4}. The same experiment was used to evaluate cross-talk between the value acquired by each storage element. No cross-talk was observed down to levels below 1 mV.

G. Radiation Robustness

Radiation robustness was evaluated by dosing an electrically biased ASIC at room temperature using 8 keV radiation at a rate of 0.9 Gy(Si)/sec. A 1.3 mm diameter pinhole was visibly aligned with the chip to select an area of dosing. A phosphor surrounding the edges of the pinhole was then used as a guide while directing the x-ray beam through the pinhole. After total accumulated dose levels of 10 kGy(Si) and 70 kGy(Si) both falling and rising transitions of the addressing registers were evaluated and the response to injected charge of dosed pixels (similar experiment to Fig. 10) was studied. Address register functionality remained at each accumulated dose level. At 70 kGy(Si) accumulated dose the readout of the signal due to injected charge was compromised. Further investigation revealed failure of the NMOS input folded cascode amplifier used to drive the stored valued out of the pixel. The Class AB amplifier was functional after accumulated dose levels of 70 kGy(Si). A 500 μm thick Si detector layer will attenuate the dose to the CMOS by a factor of 1.3×10^3 with an incident x-ray energy of 8 keV and by 5.6 with an incident energy of 13 keV.

IV. Conclusion

This article described development of an analog PAD that isolates single synchrotron bunches and accumulates in-pixel. Two switched-capacitor pixel architectures were explored to accomplish in-pixel accumulation. One uses a discrete-time integrator at the pixel back-end to allow for re-addressing and addition to storage elements. The other pixel architecture uses the front-end integration capacitors as storage elements during signal acquisition. The architecture that accumulates at

the front-end was measured to have better noise performance, lower spurious signal per accumulation, and a lower power requirement for a given settling time than the architecture that accumulates at the pixel back-end.

In terms of 8 keV x-rays the fixed ASIC read-noise was measured to be 1.07 x-rays while the noise was found to grow with the square-root of the number of accumulations at a rate of 0.19 x-rays. An improvement to the fixed detector read-noise without subsequently sacrificing detector full-well is desired. A possible approach to improve the read-noise is to implement digital full-well extension techniques, which would allow an increase in the front-end charge-to-voltage gain without sacrificing full-well [17]. Digital extension techniques remove charge from the front-end integration capacitor and increment an in-pixel counter when the front-end output passes a threshold. At exposure end, the pixel output is the combination of the counter value and an analog residual. However, an extension technique will only be acceptable if the minimum time resolution is not sacrificed.

The detector was found to respond linearly to injected charge of up to 1880 8-keV x-rays (660 fC) into a single frame element. Unfortunately, only about one-half of the supply voltage is used for signal acquisition due to limited amplifier swings and switches with p-n junctions that forward bias during certain holding configurations. Techniques that increase the supply voltage utilization and subsequently raise the saturation value will be pursued. First, switch type and architecture (ie, switches on the sides of both plates of capacitors) will be more carefully chosen. Further, since CMOS transistor reliability depends on relative voltages between terminals rather than absolute voltages, over-driving certain switches may expand the usable voltage range of the pixel without risking damage to the transistors [18].

Radiation robustness was measured and pixel functionality remained after accumulation of 10 kGy(Si). However, after 70 kGy(Si) pixel functionality was lost. Higher radiation tolerance is desired. Investigations of the prototype ASIC radiation failure mechanism will be undertaken and changes made to improve radiation tolerance.

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