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Authors(s): Hugh T. Philipp, Lucas J. Koerner, Marianne Pouchet, Mark W. Tate, Sol M. Gruner, Cornell Univ.

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First results from the 128×128 pixel mixed-mode Si x-ray detector chip (Paper Presentation)

Paper 6706-29 of **Conference 6706**

Authors(s): Wayne Vernon, Matt Allin, Ron Hamlin, Tom Hontz, Doan Nguyen, Area Detector Systems Corp.; Xuong Nguyen-Huu, Univ. of California/San Diego; Frank L. Augustine, Augustine Engineering; Sol M. Gruner, Daniel R. Schuette, Mark W. Tate, Lucas J. Koerner, Cornell Univ.

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First results from the 128x128 pixel mixed-mode Si x-ray detector chip

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ABSTRACT

A Mixed-Mode Pixel Array Detector has been developed to measure protein crystallographic diffraction patterns. X-rays are stopped in a 500 μm thick layer of silicon diodes, and collected charge is processed by an attached ASIC. Goals of the project are high flux (10^8 x-rays/s/pixel) capability and fast readout (< 0.5 ms dead time between frames). "Mixed-Mode" refers to a readout method whereby integrated signal accumulating in each pixel is compared against a threshold value. When the threshold is reached, a digital count is added to an 18-bit in-pixel counter and a set quantity of charge is removed from integrator. At the end of the x-ray exposure, analog signal left in the integrator is separately processed. Thus, one obtains mixed digital and analog data where the counter bits are a high order word and the analog residual provides higher precision. Typically, each count is equivalent to 100 10 keV x-rays, for a well-depth $>10^7$ 10 keV x-rays/pixel. The analog residual is digitized to 9-bit precision allowing measurement of the residual charge to better than a quarter of the charge from single 10 keV x-rays. Measurements are presented on x-ray tests at the Cornell High Energy Synchrotron Source (CHESS). Dynamic range, linearity, point-spread function and noise properties are shown. Status will be is reported on five different approaches for ASIC-diode hybridization. Progress toward bonding of a 128 x 512 pixel device is also presented.

Keywords: x-ray, detector, MMPAD, pixel, silicon

1. INTRODUCTION

Pixel Array Detectors (PADs) for x-ray measurement present the opportunity to improve the readout time, point-spread function, temporal resolution, dynamic range and signal-to-noise ratio with respect to CCD-based detectors currently in use at synchrotron beam-lines [1-5]. A PAD consists of a fully-depleted semiconductor diode layer where incident x-rays are converted to charge carriers and a CMOS readout chip that processes the charge, electrically coupled to the detecting layer via bump-bonds at each pixel. A collaboration between Area Detector Systems Corporation (ADSC) and Cornell Pixel Array Detector Group has been developing a Mixed-Mode PAD (MMPAD) with a pixel optimized for macromolecular crystallography applications.

Recently, full-sized CMOS readout chips and high-resistivity detector layer chips have been received. Work is ongoing to produce and characterize detector hybrids and develop custom off-chip control and data acquisition electronics. At this time two MMPAD prototype detectors have been developed and are in active use. The first is a single chip prototype built for the express purpose of studying the performance of the MMPAD detector hybrids. To this end it relies on off-the-shelf test electronics for its control and data acquisition. The second prototype is a two-by-four array of detector hybrids, *i.e.* eight total detector hybrids. The purpose of this prototype is primarily to support the development of a compact, custom off-chip electronics system that will be used in the final, large area detector.

In this paper we present preliminary test results from the single chip prototype using laboratory x-ray sources and the Cornell High Energy Synchrotron Source (CHESS) F2 beamline, including dynamic range, point spread function, linearity and noise characteristics. Detector applications shown include fine phi-slicing of a crystallographic dataset and Wide-Angle X-ray Scattering (WAXS) from an aluminum sample that includes the unsaturated measurement of the direct CHESS beam. We report on the development of self-contained detector modules that are intended to become the

building blocks of the ultimate, large area detector. Finally, we conclude with a discussion of detector hybridization schemes investigated by our collaboration.

2. SYSTEM DESCRIPTION

The design goals of the mixed-mode detector are summarized in Table I.

TABLE 1: DESIGN GOALS FOR THE MIXED-MODE DETECTOR

Pixel Size	150 x 150 μm^2
Detector format	2048 x 2048 pixels
ASIC Size	128 x 128 pixels
Integrator well-depth	100 x-rays (10 keV)
Digital counter depth	262144 (2^{18})
Overall well-depth	2.6×10^7 x-rays
Maximum count rate	10^8 x-rays/s
Minimum count rate	< 1 x-rays/s
Readout Dead Time	< 0.5 ms
Systematic Error Limit	0.25%
X-ray Energy Range	5.9keV to 15keV

2.1 Pixel Design

A thorough discussion of the motivation for and evolution of the mixed analog and digital approach can be found in [3]. Here we only present a brief review of the key features distinguishing the Mixed-Mode PAD from other area x-ray detectors. Most area x-ray detectors currently in use at synchrotron x-ray sources accumulate the x-ray signal during an exposure in an analog element, *e.g.* the charge well of a CCD, then digitize it during the period between exposures. Optimization of the detector sets the noise and settling time constraints within the analog output chain and analog-to-digital conversion circuit such that further optimization tends to trade-off between readout speed, precision and well-depth. The Mixed-Mode PAD avoids this trade-off by performing the high order quantification *in-situ* with the exposure, leaving only a small analog residual to be digitized following the exposure.
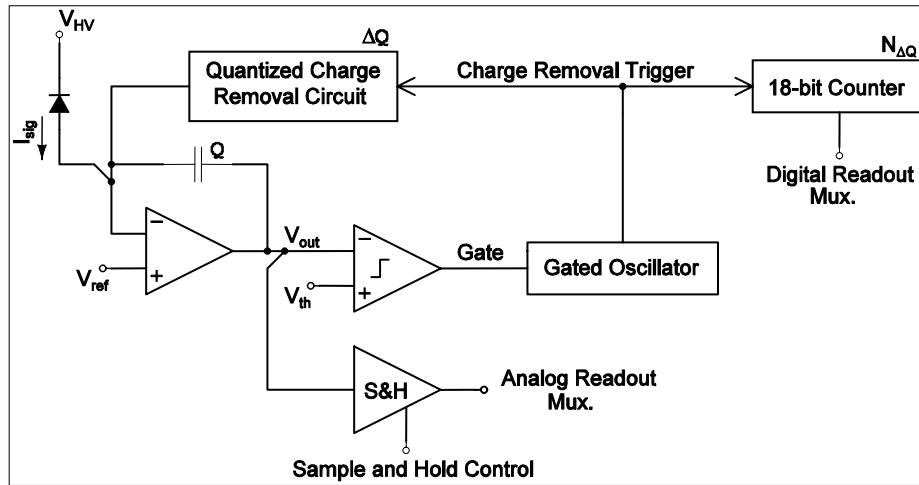

Fig.1. Illustration of the Mixed-Mode PAD pixel circuitry.

Figure 1 provides a high level illustration of the MMPAD pixel circuitry. The basic concept of this design is to accumulate the diode's current signal (I_{sig}) as a charge (Q) stored in the analog integrator. As charge accumulates the voltage at the integrator's output node (V_{out}) slews downward until it falls below the comparator threshold (V_{th}) activating the gated oscillator. Every cycle of the oscillator causes a set quantity of charge (ΔQ) to be removed from the

integrator and increments the 18-bit counter that records the number of charge removal operations ($N_{\Delta Q}$) preformed. When the detector is read out the number of charge removal operations ($N_{\Delta Q}$) and integrator's output voltage (V_{out}) are recorded. With this information it is possible reconstruct the total x-ray signal via the relation:

$$N_x = \alpha \cdot (\beta \cdot N_{\Delta Q} + Vout - V_0),$$

where N_x is the number of x-rays measured, α and β are scaling factors, and V_0 is a constant zero-point offset correction.

By *in-situ* digitization of the highest order data, the analog-to-digital conversion precision required of the analog residual voltage (V_{out}) is reduced to only 10-bits. This can be accomplished with commercial electronics as rates well beyond 50 MHz and therefore substantially above our requirements. The digital data ($N_{\Delta Q}$) may then be read out at very high rates, *e.g.* 50 to 100 MHz. In this way the MMPAD is capable of simultaneously achieving very short readout times at better than single 10 keV x-ray precision with a well depth that is orders of magnitude larger than what is commonly found in the current generation of synchrotron area x-ray detectors. Quantitative measurement of these aspects of the detector prototype's performance are presented in section 3.

2.2 Module Design

The ultimate goal of the MMPAD project is the fabrication of a large area, 2048 x 2048 pixel detector. Because of size limits in integrated circuit fabrication, this will require the tiling together of 256 (16 x 16) 128 x 128 pixel detector hybrids. To make this task tractable we are developing a 128 x 512 pixel module, consisting of four detector hybrids, that will form the basic building block of the large area detector. Each module will be self-contained, with custom control and data acquisition electronics as well as an integrated system for maintaining the thermal fidelity of the detector hybrids. Developing the module design is quite an involved task due to speed and signal integrity requirements as well as the high level of system integration. In section 4 we report on the design and construction of a prototype module and present a 256 x 512 pixel Mixed-Mode PAD prototype composed of two prototype modules.
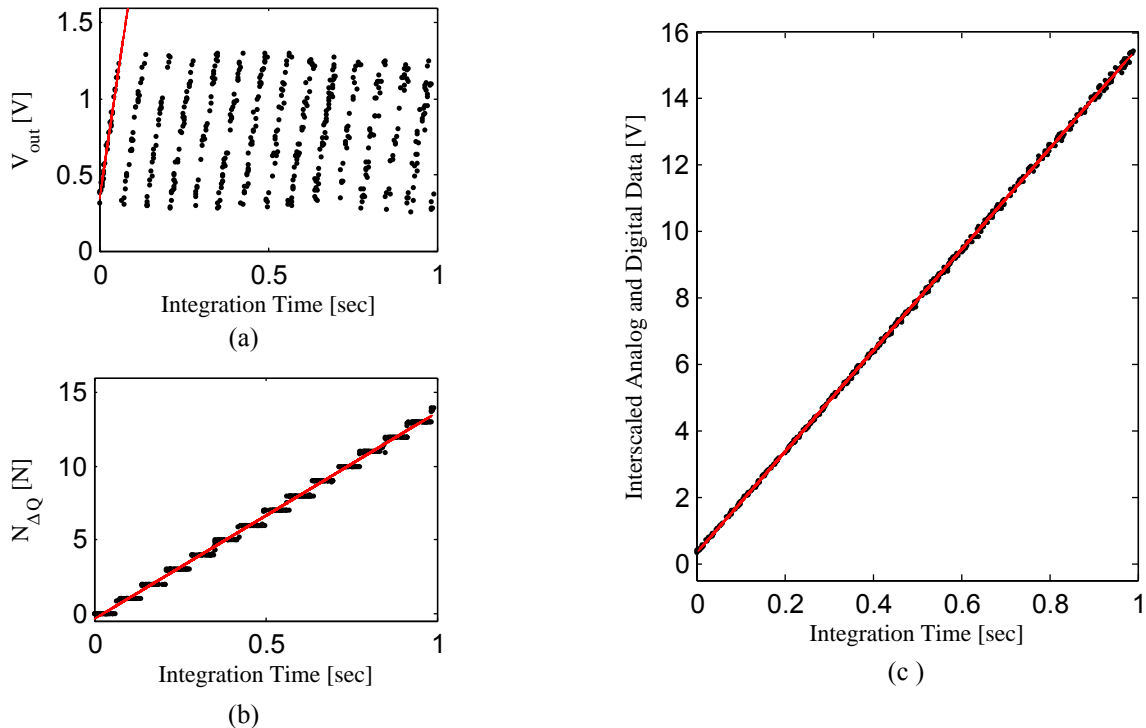

Fig.2. Panels (a) and (b) depict, respectively, the analog and digital data from one pixel, obtained from a large number of independent, constant source exposures, taken with exposure times varying from 100 μs to 1 s and averaged over 25 repetitions. A line has been fit to the first integration cycle of the analog data and the entire digital data to illustrate linearity. Panel (c) shows the combined data, where a constant scale factor has been applied to the digital data to merge it with the analog residual. Also shown is a best-fit line to demonstrate the linearity of the combined data.

3. PRELIMINARY TESTING

Evaluation of these chips has been underway since early April 2007 with two experimental runs at the Cornell High Energy Synchrotron Source (CHESS) completed, as well as testing with laboratory rotating anode, x-ray tube, and radio-nucleotide sources. Analysis of this data and optimization of the detector is still underway. Therefore the results presented here should be considered preliminary, representing the worst-case performance of the final MMPAD detector.

3.1 Detector Well-Depth and Linearity

The combination of analog and digital data in the MMPAD allows for a large total well-depth while simultaneously allowing a high maximum input flux per pixel. As discussed in section 2.1, the MMPAD combines 18-bits of digital data with the well-depth of an analog charge collector. The well-depth of the analog collector is a variable parameter that may be set within a range of 1 to ~150 10 keV x-rays. Typically we have operated with a setting equivalent to ~100 10 keV x-rays. This configuration yields a total system well-depth of more than 2.6×10^{7} 10 keV x-rays. The speed of the pixel circuitry is designed to allow a minimum quantized charge removal rate of 1 MHz which corresponds to a maximum input flux of at least 10^{8} 10 keV x-rays/pixel/s.

To test the system linearity we must independently confirm: (1) the linearity of the analog charge collector's charge to voltage conversion, (2) the linearity of the charge removal quantifier, and (3) the accuracy of the calibration factor used to scale these two portions of the data. The first two points were checked independently using a constant current source. Figure 2 shows the resulting analog and digital readings from a series of separate integrations, acquired in a random order to remove source systematics. In addition, figure 2 shows the complete scaled results for a typical pixel.
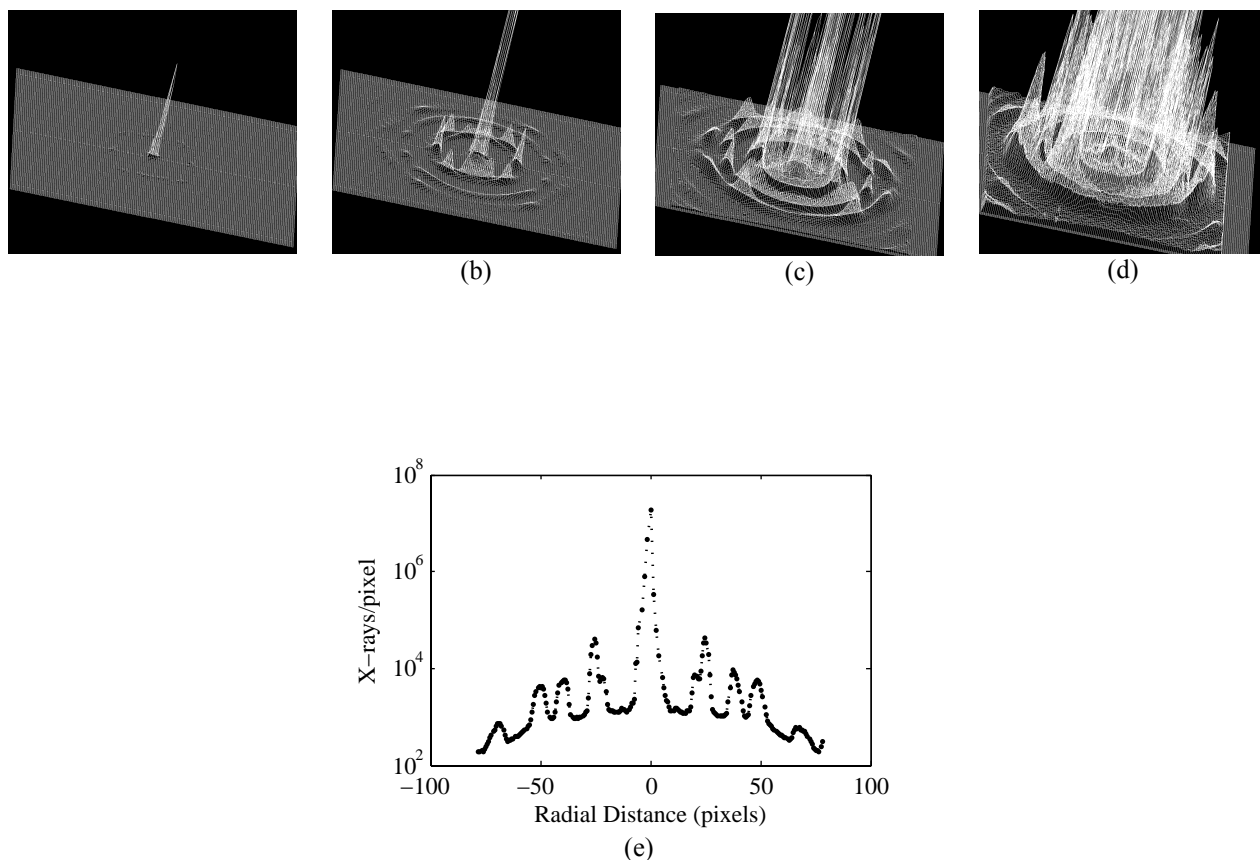
(b)   (c)   (d)

(e)

Fig.3. A wide angle diffraction data set from a thin Aluminum sheet is shown at increasing intensity scales from image (a) to image (d) An angular profile of this data is shown in panel (e); note the vertical axis is logarithmic. The data set was acquired in a single, 1 s exposure and clearly illustrates the large dynamic range of the MMPAD. Both the signal of the attenuated main beam (shown in image (a) with a peak flux of ~18 million x-rays/pixel/sec) and the sixth order ring (shown just inside, though not at, the edge of images (c) and (d) or as the 5th peak from the center in panel (e) with a peak flux of ~700 x-rays/pixel/s) are clearly visible and measured with good statistics although they differ in intensity by a factor of more than 25,000. The dynamic range of the MMPAD is, in fact, larger than this example would suggest, as even fainter rings should also be observable with a larger area MMPAD detector.

To demonstrate the performance of the MMPAD under extreme flux conditions near the limits of its design specifications a single, one second, exposure of 1/32" sheet of aluminum was taken, with no beamstop, at the CHESS F2 beamline. The resulting diffraction pattern is shown in figure 3 on four different intensity scales. The central pixel has an x-ray flux of nearly one quarter of the MMPAD design limit. This allowed us to measure, in a single exposure, values that spanned nearly the entire well-depth of the detector. In this pattern the brightest pixel, located in the image of the direct beam at the center of the pattern, recorded more than 1.8×10^7 x-rays while in the sixth order diffraction ring, visible at the highest level of magnification, the brightest pixel reports only ~700 x-rays. The intensities recorded by these two pixels differed by more than a factor of 25,000, which notably is larger than one third of the total well-depth of typical phosphor coupled CCD x-ray detectors, and yet with a larger area detector it should have been possible to see even fainter rings.
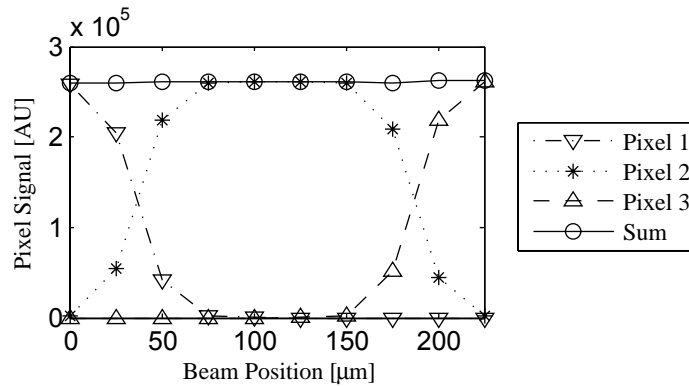
Fig.4. Translation of a 25 μm spot across three pixels, illustrating the sharing of charge between a pixel and its neighbors at and near the pixel boundary. While charge may be shared between pixels in the boundary region, no charge is lost since the summed charge remains constant.

3.2 Detector Point Spread and Charge Sharing

The typical point spread function of a phosphor coupled CCD detector extends substantially beyond the limits of the boundary of a single pixel with a power law decay that covers many pixels [6]. Although this can be beneficial in determining the centroid of well-isolated diffraction spots, it makes it very difficult to measure weak diffraction spots that are in close proximity to bright ones. Fully depleted PAD detectors, on the other hand, have a point spread that is limited to the extent of the pixel, as shown in figure 4, which depicts the translation of a 25 μm spot across a three pixel neighborhood. The signal accumulated in each pixel is shown with some sharing of the signal between neighboring pixels when the spot is near or overlaps the pixel boundary.

The curve shown in figure 4 agrees with the convolution of the beam size and shape with the expected 10 to 15 microns of charge spreading within the detector layer.

3.3 Noise Performance

The noise statistics of a mixed-mode detector differ in important ways from more traditional area x-ray detectors because of the *in-situ* digitization of the x-ray signal that occurs via the charge removal operations. Generally we may distinguish between two noise categories in a mixed-mode detector: (1) fluctuations in the analog residual voltage, measured once during the analog-to-digital conversion during detector readout, and (2) the quantization error introduced with each charge removal operation. The first noise source is analogous to the sources one finds in CCDs and is discussed at length in [7]. The uncertainty introduced by the charge removal operation is fundamentally different from the digitization of the analog residual. Characterization of this quantization noise is still in progress and therefore will not be presented here; however, we briefly discuss why this noise source is different.

A detailed analysis of the noise in the MMPAD analog residual voltage entails consideration of the pixel front end design, the analog buffer and multiplex system which coveys signals off chip to the point of digitization, as well as the digitizers themselves; as such it is beyond the scope of this paper. However, a simple end-to-end measurement of this noise may be obtained by calculating the difference of two dark field images taken under identical conditions. Figure 5 shows such a measurement for the working pixels on a single chip at 18 C. Assuming normal noise, the standard deviation of this data should be $\sqrt{2}$ times the RMS of the analog system's noise. In this case, the standard deviation of the data was 6.4 mV which yields an analog residual voltage noise of 4.5 mV. Since a 10 keV x-ray results in a ~10 mV shift in the analog residual voltage, the signal-to-noise ratio of the MMPAD prototype at this temperature is at least 2. Simulations of the ASIC and studies of the detector prototype indicate that this noise is dominated by the read out chain off-chip and ADC ground-bounce error. It is expected that the analog residual noise voltage will fall below 1 mV with the integrated ADC readout electronics being developed for the final detector.
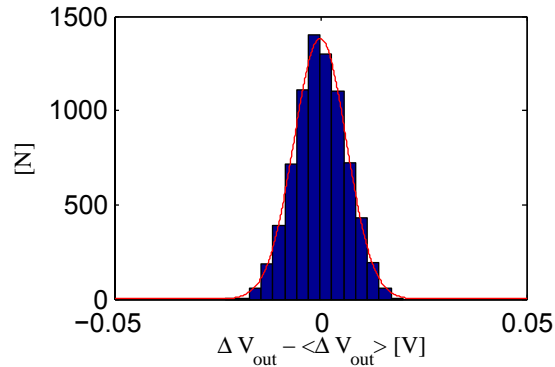
Fig.5. Histogram of the difference in pixel readings (V_out) from two successive 100 μs dark field exposures along with a Gaussian fit to this data. From the Gaussian fit the standard deviation of this distribution is found to be 6.4 mV, yielding a single measurement error of 4.5 mV.

The primary factor that distinguishes the charge removal quantization noise from that more typical in other area x-ray detectors is that it results from a repeated, typically periodic, sampling process rather than a single measurement. Therefore, its interaction with the spectrum of noise in the pixel is different in that periodic noise at frequencies near the rate of charge removal operations, as well as higher order harmonics, will be selectively sampled in a constructive fashion. Because of this measurement of the noise introduced by the quantifier can vary notably, depending on the conditions under which the data is taken. Preliminary data suggests that this noise contribution is low, however further measurements and analysis are needed for a robust characterization.

3.4 Readout Dead Time and Frame Rate

One of the most important characteristics of the MMPAD is the higher frame rate of the detector. Most x-ray detectors (*e.g.* phosphor coupled CCDs, image plates) digitize values stored in some type of analog element during the readout phase. This approach creates a trade-off between speed, well-depth, and accuracy, resulting in typical frame rates slower than 1 Hz. The MMPAD, however, digitizes the highest order data portion of the data *in-situ* with each exposure producing digital data ($N_{\Delta Q}$) that may be read out at high speed and an analog residual (V_{out}) that only needs to be quantified with 10-bit accuracy. This makes it possible to achieve pixel readout rates beyond 4 million pixels per second, in turn permitting full detector readout in 0.5 to 1.0 ms with only a small number of parallel output channels.

Not surprisingly much of the challenge in achieving these data readout rates is in developing off-chip support electronics that are capable of maintaining signal integrity at these very high speeds. Currently the single chip mixed mode prototypes has been successfully operated with readout dead times of less than 5 ms. The speed limit in this system is imposed by the off-the-shelf test electronics used to control the detector chip. As we will discuss in section 4, work is underway to develop a tightly integrated detector module, with custom control and data acquisition electronics located very near to the detector hybrids, that should be capable of operating at a much higher readout speed. Currently the prototype module had been operated with a readout dead time of 1.5 ms, however with careful tuning of the control and data clock edge timing we anticipate achieving a final readout dead time of between 0.5 and 1.0 ms.
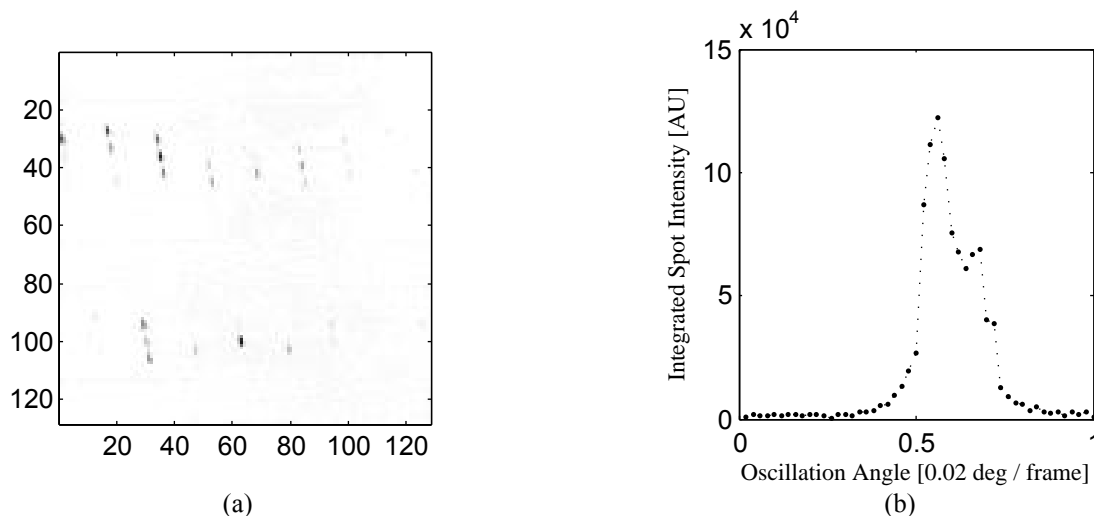
Fig.6. Panel (a) shows a section of a protein crystal diffraction pattern (Thaumatin) taken in the canonical manner of a single, long exposure during which the crystal is rotated through a fixed oscillation angle. In contrast, panel (b) shows the intensity profile of one of the diffraction spots from (a) acquired by continuously framing the MMPAD detector during crystal rotation.

The practical advantage a high frame rate is illustrated in figure 6 that depicts a portion of a diffraction image from a Thaumatin protein crystal. Figure 6a shows a one degree, ten second oscillation taken by a MMPAD detector in a manner typical to what would be used to acquire a CCD data set. However figure 6b illustrates the additional information that is available with from MMPAD detector. In it the one degree, ten second oscillation is divided into fifty successive frames taken as the crystal was continuously rotated and the integrated intensity of a single spot is plotted as a function of the crystal oscillation angle. This method improves he signal-to-noise ratio by reducing the accumulated background scatter to the true peak width. Furthermore, by acquiring data as the crystal rotates continuously systematic errors due to synchronization errors between the x-ray shutter and the crystal rotation axis stage can be reduced.

4. LARGE AREA DETECTOR

The first step towards building a large area detector is constructing a module from 4 hybrids in a 1 x 4 array. An initial approach has been to fabricate four separate single ASIC/diode hybrids and then position them on a substrate to form the 1 x 4 detector. Work is underway to assemble the next generation of 1 x 4 that will start with a large, monolithic diode array (128 x 512 pixels) with four ASICs bonded per diode. The 1 x 4 detector hybrids are attached to a printed circuit board (PCB) that contains all support electronics necessary for operation of the detector. These prototype modules are designed so that two may be abutted to form a 256 x 512 pixel Mixed-Mode PAD.

The 1 x 4 prototype module is self-contained in that only one cable, including a 12 V power source, connects to the outside world. A separate PCB, called the *Hub Controller,* connects up to four modules and provides an Ethernet link to the next level of the control and data acquisition system. Software commands come to the Hub Controller from a host computer and are distributed to the appropriate modules. This is the path for data files that configure the two major features of the ASICs; pixel control register (PCR) and digital-to-analog converters (DACs). Local digital control and data collection functions are controlled by an FPGA on each 1 x 4 prototype module.

A photograph of the 2 x 4 prototype MMPAD is shown in figure 7. All power supplies, including a 250 V diode bias supply are contained on the boards. Local control of the bias and guard ring voltages is provided by a DAC on each board. Some additional power supplies are necessary to provide isolation between analog and digital functions and to provide noise-free power to the analog side of the ASIC. One of the difficulties of the Mixed-Mode approach is the feed-through of digital noise to the analog chain, especially during high speed readout. Having all power functions close to the ASICs partially alleviates this problem. It is also helpful to keep signal lines short and placed in close proximity to copper planes. Each module has massive parallel readout consisting of the 32 lines of 100 MHz serial digital data and 32 lines of analog signals (up to 20 MHz bandwidth). The digital bit stream and the subsequent analog-to-digital

conversions of 10 bits/pixel are stored for one frame in the FPGA and passed to the Hub Controller during the rest of the data acquisition cycle.

Initial tests with the 2x4 prototype shown in figure 7 indicate that all the critical board functions operate as intended. The boards were recently assembled, however, and as of this writing there has not been time to perform a detailed characterization.
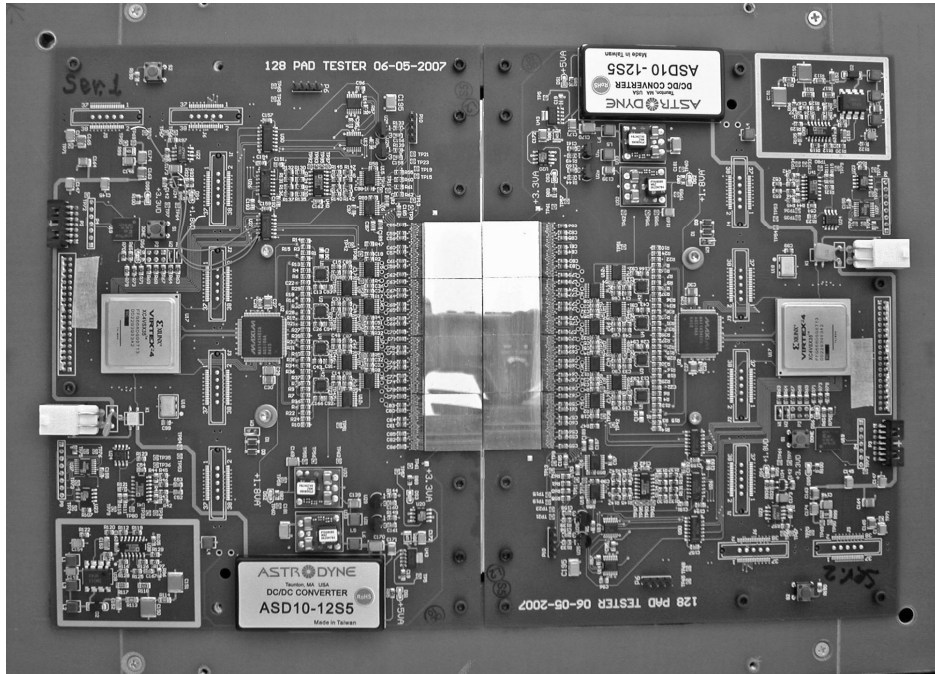

Fig.7. Photograph of the 2x4 prototype MMPAD detector. Two 1x4 prototype assemblies have been placed edge to edge; each assembly is an independent detector on a 6"x8" printed circuit card. The 8 ASIC/diode hybrids are located in the center, and the highly reflective surfaces are the aluminum cathode (x-ray entry side) of the diode array. The largest of the supporting electronics packages are Xilinx Virtex-4 SX35 field programmable gate arrays (FPGA). An 8-channel Analog-to-digital converter (MAXIM) is in the center of each 1x4 assembly. External communications and 12 V power come through the 40-pin connector on the left (or right) edge of the assembly.

TABLE 2: DETECTOR HYBRIDIZATION SCHEMES

Scheme	Applied Bump	Contact Material	Contact Method	Process Level
1	Au Ball	Silver Paste	Dipping	Chip/Wafer
2	Au Ball	Silver Paste	Screened	Chip
3	Au/Ni Bump	Silver Paste	Screened	Wafer
4	Solder Ball	Solder	Machine Attached	Chip/Wafer
5	Solder Ball	Solder	Deposited	Wafer

5. HYBRID FABRICATION

Our collaboration has been reviewing various bump-bonding schemes to connect ASICs to diode chips. A major consideration for process selection is the ability to hybridize a long diode chip by attaching multiple ASICs, *e.g.* a 1 x 4 hybrid (figure 7). These larger hybridized detectors would then be tiled to form a 2048 x 2048 pixel array with an active area of about 320 mm x 320 mm. The process must lend itself to ease of assembly while maintaining a high yield of

pixel interconnects, with high reliability, and at acceptable cost. The review below is to establish the best manufacturing process. Five methods of bump-bonding were considered, as detailed in table 2.

Scheme 1. Gold balls were attached to the ASIC using thermo-sonic bonding techniques both at the chip (3 mm x 3 mm, 16 x 16 pixels and 20 mm x 20 mm, 128 x 128 pixels) and wafer (8 inch) levels. The pads on the ASIC are Al at 50 μm square resulting in a ball size of 60-80 μm diameters. The balls, at the chip level, were flattened to a +/- 2 μm level at 35μm high. The balls at the wafer level were automatically placed by a wire bonding machine that coined or flatted the balls at +/- 4 μm at 30 μm high. The balled ASIC was then placed on a bump bonder and sequenced by dipping into a controlled level of silver paste and then aligned to the applicable diode and placed. Following placement the assembly (hybrid) was then baked at 175 C for two hours in a nitrogen environment. This resulted in excellent bond strength and good electrical contact. However yields were not repeatable and the process was not easily adaptable to the larger chip size (20 mm x 20 mm).

Scheme 2. The ball placement is the same as in Scheme 1 but the ASIC was not dipped into silver paste. In this scheme silver paste was screened onto the diode pads. These pads were gold surfaced and larger than the ASIC pads at 90 μm square. Again this resulted in excellent bond strength and good electrical contact. Difficulty in achieving consistent yields resulted from apparent sliding of the ball contact during placement.

Scheme 3. Wafers (containing 60 whole ASIC chips) were submitted to an electro-plating technique that builds up 35μm Ni on each 50 μm pixel pad and then thinly gold plated. The chips were separated from the wafer by standard sawing techniques and then bump bonded to the diode chip. The diode chip pads were screened with silver paste the same as in Scheme 2. The result was excellent bond strength and good electrical contact. Yield on contacts was high and quite acceptable.

Scheme 4. An ASIC wafer was prepared by changing the standard Al pad to a gold contact pad. The wafer was then sawed into individual chips (20 mm x 20 mm). Solder balls (80 μm diameter) were then individually placed on each pixel pad; and were deposited on each individual chip by an automatic placement machine. Placement was accurate and yield (no missing balls) was close to 100%. Using a flip chip assembly machine the ASIC chip was then solder-bumped to a diode array. The result was excellent bond strength, good electrical contact and high pixel contact count.

Scheme 5. Presently in process is an ASIC wafer that is being prepared with solder ball deposition that will be sawed into individual chips. These chips will then be bump bonded to a long diode that will accept 4 individual ASIC's using a conveyer oven soldering technique.

The silver paste approach has the advantage of low temperature processing and requires no flux. However, placement is not forgiving and requires an accuracy of at least 2 μm. It also creates in a potential yield problem, as repairs are not possible. This approach does not lend itself to ease of multi-ASIC on diode array assembly, and compared to soldering techniques it is more costly.

The solder ball bumping described as scheme 4 proved to be effective in ball-bumping attachment and lends itself to multi-ASIC chip to diode hybridization. Advanced "no clean" fluxes were evaluated and found to be acceptable. The strength of the bonding achieved was sufficiently strong as to obviate need for additional adhesive filling agents. Scheme 5 is still being evaluated. Its purpose is to determine yield and cost advantages over the discrete chip approach.

6. FUTURE PLANS

The goal for the detector is a 2048 x 2048 pixel array. Results summarized herein demonstrate the viability of the MMPAD strategy and document the fabrication of appropriate hybrid detectors. The next step will involve tiling hybridized chips to cover a larger area in a 2048 x 2048 pixel format and development of suitable calibration procedures. Standard CMOS fabrication limits each ASIC to 128 x 128 pixels, so to facilitate this tiling the 1 x 4 module prototype described here will be re-configured into a package that allows close packing. Four modules will then be put together to make a 512 x 512 pixel unit and 16 units combined make a 2048 x 2048 pixel MMPAD. The relatively high data rates coming from the four chips of the module will be handled by a field programmable gate array (FPGA) that moves 32 high speed digital serial lines from the ASICs to short term memory at about 500 Mbyte/s. After the 0.5 ms readout time, the FPGA will move the data to the next level of the data collection pyramid at a more leisurely rate during acquisition of the next frame. The last stage of the data collection pyramid is a set of Ethernet cables going to a network

switch. Present planning calls for 16 cables of gigabit/s Ethernet to carry the approximately 0.12 Gigabit of data for each frame. However many more testing and evaluation steps are needed to fully characterize this new detector, and the work is ongoing.

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