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Development Of A Pixel Array Detector For Time Resolved X-ray Imaging

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Abstract. We are developing an integrating Pixel Array Detector (PAD) for microsecond time-resolved x-ray diffraction. The current detector prototype has a format of 92x100 pixels, each 150 μ m square, and covers an active area of 15x13.8 mm². The detector was tested at the CHESS D1 beamline and imaging capabilities within the microsecond time resolution regime were successfully demonstrated. This prototype is a test module en route to a larger detector of 1000x1000 pixels suitable for dedicated operation. Areas in need of improvement (radiation-hardness, large area coverage) will be discussed.

INTRODUCTION

Intense synchrotron sources now deliver sufficient x-ray flux to enable very rapid time-resolved studies of dynamic materials, such as enzyme-substrate interactions, contracting muscle, polymerization, materials failure, elastic deformation under stress, and field-induced changes in liquid crystals (1-4). Typically, the factor most limiting the execution of these experiments is the absence of imaging detectors capable of quantitatively recording the data at the required rate (1 ns – 100 ms per frame). While charge-coupled device (CCD) detectors have greatly expanded the range of experiments that can be performed on slower (> 100 μ s) time scales, limitations inherent in CCDs and phosphors preclude framing at very high speeds.

The Pixel Array Detector (PAD) is a flexible technology with the potential to both perform very fast x-ray detection and to overcome the limitations of CCD-based devices. A PAD consists of a pixellated semiconductor diode layer, which directly converts the x-rays to charge carriers, bump-bonded to a pixellated CMOS electronics layer, which processes the carriers generated. Bump-bonding allows a 100% fill-factor. Each pixel-diode has its own processing electronics, thereby offering a high degree of parallelism and flexibility in the design of the electronics. Three broad categories of semiconductor array detector are currently under development: photon integrating PADs, photon counting PADs (5) and arrays based on amorphous silicon (6). This article describes x-ray tests of a 92 X 100 pixel prototype detector, which is

part of a photon integrating PAD design effort started at Princeton University and relocated to Cornell University when key personnel moved to Cornell in 1997.

THE 92 X 100 PAD

This PAD architecture was designed for on-chip frame storage capability in microsecond time-resolved experiments. The device is capable of storing up to 8 sequential frames with microsecond time resolution before pausing for data readout. Figure 1 shows the pixel schematic. Each pixel contains an integrating input amplifier, an array of 8 storage capacitors and an output amplifier. The pixel architecture and testing of small (4×4 pixel) devices have been described (7-9).

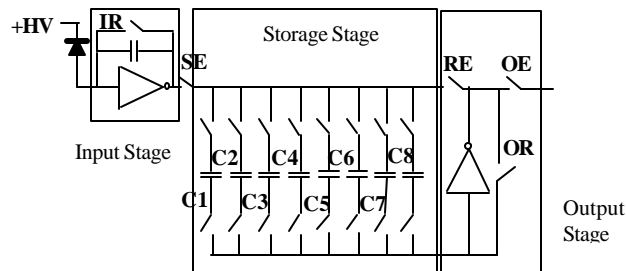


Figure 1. Electronics integrated into each pixel. Charge produced by the conversion of x-rays within the diode is integrated onto the capacitor in the input stage. Rapid imaging is accomplished by storing the integrated voltage of successive images onto one of 8 storage capacitors (C1 – C8). Digital switching logic is used to select the desired capacitor. On readout, each capacitor is connected in succession to the output amplifier which is multiplexed to a buffer amplifier at the end of each pixel row. Also shown are various pixel control switches: IR, integrator reset; SE, store enable; RE, read enable; OE, output enable; OR, output reset.

The PAD consists of a $300 \mu\text{m}$ thick high resistivity silicon layer divided into an array of 100×92 diode pixels, each $150 \mu\text{m}$ square. The active area is $15 \times 13.8 \text{ mm}^2$. The CMOS chip has 92×100 electronic pixel cells with each row of pixels connected to a buffer amplifier multiplexing onto a single serial output line for off-chip digitization. The silicon diode array was manufactured by SINTEF (SINTEF, Oslo, Norway), the CMOS chip by MOSIS (The MOSIS Service, University of Southern California, Marina del Rey, CA) using a Hewlett-Packard (HP) $1.2 \mu\text{m}$ CMOS process and bump bonding of the two layers was performed by GEC-Marconi (GEC-Marconi, Caswell, UK). Detector operation consists of two steps: an integration/storage sequence of up to eight full frames and a subsequent readout sequence. Microsecond time resolution is accomplished at the expense of the introduction of a duty cycle necessary for data read-out and digitization. The detector controller is a reconfigurable processing unit providing random logic and control signal sequencing (9,10). The integration time is externally selectable using a logic gate pulse applied to the IR switch (see Figure 1) of duration from $1 \mu\text{s}$ up to several minutes. During operation the PAD assembly is cooled at -20C within a vacuum cryostat having a light tight, x-ray transparent window. The diode layer is biased to an over-depletion voltage of $+60\text{V}$.

Out of a lot of 87 fabricated detectors, 13 detectors were randomly selected and characterized at room temperature. All but one of the tested detectors had > 99% working pixels. Three of these devices were fully characterized at -20C using a variety of input signals, including visible light, thermally generated pixel dark current, and x-rays from both a laboratory and a synchrotron source. A summary of the detector parameters is given in Table 1 of reference (10).

High speed imaging of time-varying signals.

Preliminary testing with visible light used a red He-Ne laser from a 5mW commercial pointer. For x-ray imaging, a polychromatic x-ray beam was used at the CHESS-D1 beamline. Detailed testing with a monochromatic 8.9 keV synchrotron beam is reported elsewhere (10).

The detector is sensitive to visible light as well as x-rays. For visible light imaging the light tight entrance window of the detector cryostat was replaced with a light transparent vacuum tight window. A 5mW red He-Ne laser beam was focused into an aluminum coated reflective surface mounted on the spinning head of a Dremel mill tool, which was operated at 30,000 RPM. The distance of the rotating surface to the detector diode layer was 50-60mm. This set-up produced a periodic sweep of the laser beam across the detector surface. The detector integration time was set at 25 μ s with 1 μ s of dwell time between frames. Several images were collected with no synchronization with the start point of the beam sweep. Shown in Figure 2 are images of 6 collected frames: the laser beam spot is clearly visible while it moves across the detector surface on a selected area of 21x100 pixels.

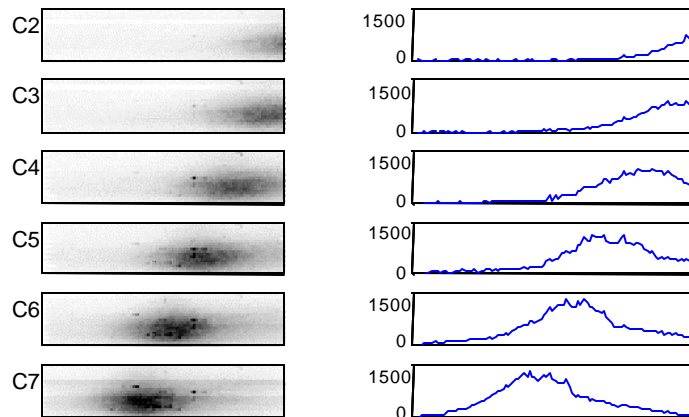


Figure 2. He-Ne Laser spot swept across the detector surface for capacitors C2-C7. Integration time was set at 25 μ sec with 1 μ sec of frame dwell time. The selected area shown corresponds to 21x100 pixels. Profiles of the peak intensity are shown on the right-hand side: the expected linear speed of about 50m/sec is correctly computed on the recorded images.

The integrated peak signal is about 1000 ADU, or the signal equivalent of 362 8.9keV x-rays/pixel. The total flux is still quite modest, limited by laser intensity and detector entrance surface reflectivity (~99%).

Time-resolved Laue diffraction tests were performed on the CHESS D1 bending-magnet beamline, which was set-up in white-beam (polychromatic) mode by removing the multilayer monochromator from the beam path. Unfortunately, the detector used for this experiment was the unit which had several percent bad pixels and the run ended before another device could be tested. Although a better device might have been selected, the essential features can still be seen. The sample in this case was a 180 mm diameter, 1.5 mm thick disk of type 3003 bendable aluminum sheet. This specific aluminum was selected for its large grain size (0.1 - 0.5 mm) which produced an intense diffraction pattern featuring radial streaked lobes of diffracted intensity (Figure 3). The disk was mounted on a circular saw with a rotation rate of 2500 RPM. The beam size was set to $1 \times 1 \text{ mm}^2$ and the sample to detector distance was 30 mm. Although high-speed framing is controlled by multiplexing signals on the PAD, a slower mechanical shutter (200ms aperture time) was additionally used to limit the detector exposure to the x-ray beam, since radiation damage was a concern.

For this experiment, an integration time of $100 \mu\text{s}$ with frame delay time of $25 \mu\text{s}$ was employed yielding 8 images/ms. Each grain from the polycrystalline aluminum sample formed its own Laue pattern over the energy range of 5 to 25 keV. The strong peaks visible in the images are the superposition of many highly oriented grains of the sample. The 8 images were obtained as the disk rotated through an angular range of 15 degrees. About 13,000 x-rays/pixel were recorded in the brightest diffraction peaks corresponding to 80% filling of the pixel well. Transmission Laue patterns on an Al-Li 2090 aluminum alloy (11,12) also shows similar radial streaks and has been used with x-ray microbeams to map the fatigue cracks that develop under too much stress.

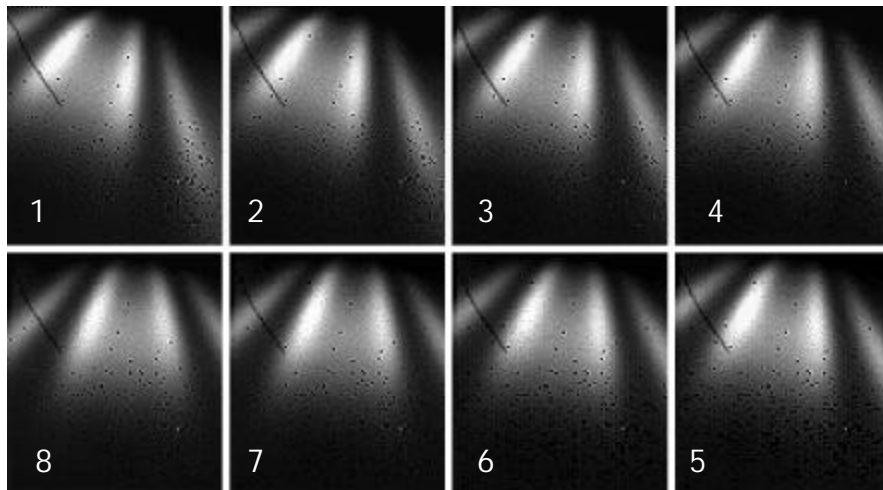


Figure 3. Laue diffraction from a polycrystalline aluminum disk rotating at 2500 RPM. A beam of size $1 \times 1 \text{ mm}^2$ impinged upon the 180 mm diameter disk *ca.* 10 mm from its periphery. Sample to detector distance was 30 mm. The peaks visible in the images are the superposition of several oriented grains in the sample. The 8 images were obtained as the disk rotated through an angular range of 15 degrees. Integration time was $100 \mu\text{s}$ per frame with $25 \mu\text{s}$ inter-frame delay. Frames are labeled in sequence from 1 to 8. Image 8 is placed next to image 1 to highlight the angular change in the diffraction pattern. The beam position was off the imaging area to the top of each frame. In the upper left of each image, one can see the shadow of the $100 \mu\text{m}$ diameter wire used to bias the front surface of the diode layer.

Even though the prototype was not designed to be radiation-hard, it was of interest to investigate radiation damage. With a flux of 3600 x-ray/pixel/ μs impinging into the diode layer at 9 keV, a dose rate of 1–3 krad/s was delivered to the CMOS gate oxide. After 300 krad (SiO_2) of total dose, the pixel well decreased by almost 20%. This was the results of damage to the pixel amplifier at the input/output stage of the pixel cell (10). In terms of number of collected diffraction images, this total dose represents about 600 exposures for a shutter speed of 200ms. Unfortunately, due to the lack of a protective shutter matching the detector exposure time (with 3600 x-ray/pixel/ μs , it takes less than 5 μsec to fill the pixel well), most of this absorbed dose was delivered to the detector electronics during the much slower read-out sequence. Clearly, rad-hard CMOS design is an essential feature of a usable PAD.

ON-GOING DESIGN CONSIDERATIONS

Tests performed with the 92x100 PAD detector demonstrated the capability of the PAD technology for microsecond time-resolved experiments. Needed improvements include radiation-hardness, a more robust electronics pixel cell, and more pixels covering a larger area.

Since PAD technology is based upon commercially available low-cost low-volume CMOS processes, the design must evolve with the available technology. The 1.2 μm HP process used for the 92x100 PAD has been recently phased out; accordingly the electronics pixel cell design has been transferred to a 0.5 μm HP process. This is a time-consuming operation requiring redesign and re-evaluation of the performance via successive fabrication runs of small-area test chips. However, the immediate benefit of a smaller feature process is a denser integration of the components, allowing a functionally enhanced pixel. For instance, our newly designed 0.5 μm pixel cell uses a more complex differential input amplifier for better power supply variation rejection and has a switchable gain structure to increase gain for low intensity/low energy signals, yet it still fits within the original footprint of a 150 μm square pixel.

The most fundamental motivation for going to a yet smaller feature size is that CMOS transistors in deep-submicron processes (0.25 μm minimum feature size) are inherently radiation-hard when appropriate lay-out techniques are adopted (13). Based on work at CERN (13), there is every reason to believe that a PAD fabricated with a deep-submicron radiation-tolerant layout will be adequately radiation-hard for practical use.

The architecture of the 0.5 μm -process test chips has been modified, as shown in Figure 4, to allow continuous framing operation. This design allows both the very rapid framing, low duty cycle mode of the older chips and a new continuous framing mode with practically no dead time. These chips are presently undergoing testing (Fall, 1999).

Our goal is to build an array of 1000x1000 pixels. This requires tiling a large area with chips, perhaps overlapping them like shingles. Since radiation hardness is an *a priori* requirement, we first plan to optimize the pixel cell design in a 0.25 μm process before building a large area detector.

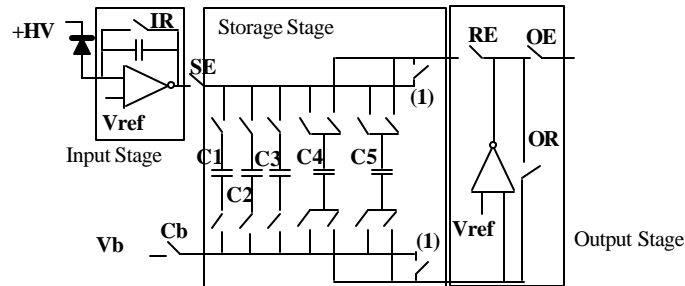


Figure 4. Electronics Pixel Cell schematic. For continuous framing operation, switches (1) are kept open and only C4 and C5 are used. In this mode, one capacitor is integrating signal while the other is read-out; after read out of the selected capacitors, the roles of the two capacitors are interchanged. When switches (1) are closed the pixel is operated for fast time-resolved using capacitor C1 to C5, similar to the mode of Figure 1. Vref is the reference voltage for the differential amplifier.

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