J. Synchrotron Rad. (1999). **6**, 1096–1105

Tests of a prototype pixel array detector for microsecond time-resolved X-ray diffraction

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(*Received 27 April 1999; accepted 19 July 1999*)

X-ray test results from a prototype 92 × 100 pixel array detector (PAD) for use in rapid time-resolved X-ray diffraction studies are described. This integrating detector is capable of taking up to eight full-frame images at microsecond frame times. It consists of a silicon layer, which absorbs the X-rays, bump-bonded to a layer of CMOS electronics in which each pixel has its own processing, storage and readout electronics. Tests indicate signal performance characteristics are comparable with phosphor-based CCD X-ray detectors, with greatly improved time resolution, comparable linearity and enhanced point spread. This prototype is a test module *en route* to a larger detector suitable for dedicated operation. Areas of needed improvement are discussed.

Keywords: X-ray detectors; area detectors; time-resolved diffraction; Laue diffraction; CMOS imager.

1. Introduction

Intense synchrotron sources now deliver sufficient X-rays to enable very rapid time-resolved studies of dynamic materials, such as enzyme–substrate interactions, contracting muscle, polymerization, materials failure, elastic deformation under stress, and field-induced changes in liquid crystals (Gruner, 1987; Moffat, 1989, 1998; Folkhard *et al.*, 1987). For many of these systems the factor limiting experiments is the absence of a detector capable of quantitatively recording the data at the required rate (1 ns–100 ms). While recently developed charge-coupled device (CCD) detectors have greatly expanded the range of experiments that can be performed on slower (>100 μs) time scales, they cannot be improved very much because of limitations inherent in the CCDs and phosphors.

This article describes X-ray testing of a prototype pixel array detector (PAD). The PAD is a flexible technology which has the potential both to perform very fast X-ray detection and to overcome the limitations of CCD-based devices. A PAD consists of a pixelated semiconductor layer, which directly converts the X-rays to charge carriers, and a pixelated electronics layer, which processes the carriers generated. Each pixel has its own processing electronics, thereby offering a high degree of parallelism and flexibility in the design of the electronics. Groups around the world are developing three broad categories of semiconductor array detectors: photon-integrating PADs, photon-counting PADs, and arrays based on amorphous silicon. PADs typically consist of a high-resistivity silicon layer bump-bonded to a complementary metal oxide semiconductor (CMOS) electronics layer. In photon-integrating devices the signal in each pixel is locally integrated for later readout (Barna *et al.*, 1995, 1997; Eikenberry *et al.*, 1998). Such PADs can accept signals at the highest count rates at the cost of a duty cycle to read out the detector. Photon-counting PADs differ in that the CMOS electronics count each photon individually (Datte *et al.*, 1999). Since the area of a pixel limits the complexity of the CMOS electronics which may be fabricated in that pixel, photon counters typically must download their counts after a number of counts have been accumulated, which ultimately imposes a count-rate limitation.

Detector arrays based on amorphous Si layers are attractive because the material can be inexpensively produced in large areas. However, amorphous Si electronics have inherently higher noise than PADs, which are fabricated on single-crystal Si (Ross *et al.*, 1997). Currently, amorphous Si detectors are being developed primarily for medical radiographic applications in which the quantitative noise performance is less critical because of the higher doses and higher-energy radiation that are used. However, amorphous Si technology is still evolving and may yet prove to be useful in various scientific applications. The

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discussion below will be confined to PADs based on CMOS electronics for scientific applications.

The direct conversion of X-rays to charge in a semiconductor has advantages of time resolution and good noise performance. For comparison, a 10 keV X-ray converting in silicon produces ~2700 electron–hole pairs, whereas the same X-ray converting in the phosphor of a typical phosphor/fiber-optic taper/CCD detector yields 5–30 electron–hole pairs in the CCD (Tate *et al.*, 1997). The light-emission physics in phosphors is complex and limits most phosphor CCD detectors to millisecond time resolution; in contrast, electron–hole pairs produced by an X-ray stopping in a semiconductor can be collected in nanoseconds. The primary obstacles to the development of PADs are integrated circuit-related engineering issues, as opposed to the fundamental physics and materials issues of phosphor luminescence, low-level signal performance and fiber-optics fabrication that impede CCD detector development.

Aside from speed, the most significant advantage of PADs is that the technology readily lends itself to customization for specific X-ray applications. The engineering issues that must be solved in making large area PADs include packaging, radiation damage, large area coverage and device yield. Solutions to these problems will be common to both integrating and photon-counting PADs, since these differ primarily in the electronics on the CMOS layer. However, once these problems are solved, it is straightforward to customize the detector by modifying the electronics. In practice, the CMOS designs are developed on computer workstations using industry-standard integrated circuit design tools and the resultant instructions are e-mailed to a silicon foundry for fabrication. Once the PAD detector packaging and design infrastructure is in place, making PADs customized to completely different functions does not entail totally different hardware. The off-detector electronics may change, but this typically involves assembly of off-the-shelf components. For example, we have considered PAD designs in which the CMOS pixel electronics are varied to include charge integrators, photon counters, time-autocorrelators, local background subtracting electronics and difference analyzers, with no other change in the detector chips than the CMOS fabrication instructions sent to the silicon foundry.

This article is effectively a progress report on an integrating PAD effort which was started at Princeton University and relocated to Cornell University when key personnel moved in 1997. PAD detector development proceeds by iterative cycles of device fabrication at successively larger scales. The pixel architecture and testing of small (4 × 4 pixel) devices have been described (Barna *et al.*, 1995, 1997; Eikenberry *et al.*, 1998). This article describes the first X-ray tests of a larger detector with a 92 × 100 pixel format.

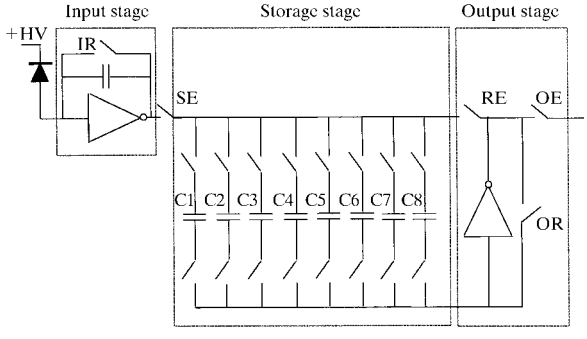

Figure 1
Schematic of the pixel structure. Shown are the electronics integrated into each pixel within the PAD. Charge produced by the conversion of X-rays within the diode is integrated onto the capacitor in the input stage. Rapid imaging is accomplished by storing the integrated voltage level from successive images onto one of eight storage capacitors (C1–C8). Digital switching logic is used to select the desired capacitor. On readout, each capacitor is connected in succession to the output amplifier which is multiplexed to a buffer amplifier at the end of each pixel row. Also shown are various pixel control switches: IR, integrator reset; SE, store enable; RE, read enable; OE, output enable; OR, output reset.

2. Detector description

The PAD described below was designed for on-chip frame storage capability for microsecond time-resolved experiments. The device is capable of storing up to eight sequential frames with microsecond time resolution before data readout and has an adjustable exposure time ranging from 1 μs up to many seconds.

The PAD has a high-resistivity silicon layer, patterned with a two-dimensional array of X-ray sensitive diodes, each of which is solder bump-bonded to a pixel of storage and readout electronics in the CMOS layer. The silicon diode layer is 300 μm thick, covers an active area of 15 × 13.8 mm^2, and was manufactured by SINTEF (SINTEF Electronics and Cybernetics, Blinden, Oslo, Norway). The layer is divided into an array of 100 × 92 pixels, each 150 μm square. Surrounding the perimeter of the active diode area is a 150 μm-wide guard ring to minimize edge leakage currents. The CMOS chip was fabricated by the MOSIS service (The MOSIS Service, Information Sciences Institute, University of Southern California, Marina del Rey, CA, USA) with a Hewlett-Packard 1.2 μm process featuring a linearized capacitor and two metal layers for interconnections and was bump-bonded to the silicon diode layer by GEC Marconi (GEC-Marconi, Caswell, UK). The chip is electrically organized in 46 columns and 200 rows to facilitate bussing of switch select lines. Each row has a buffer amplifier multiplexing onto a single serial output line for off-chip digitization. The chip has 145 wire bonding pads, of which 30 are digital control pads, and 115 analog/digital power supply and ground connections. The clearance between the bonding pads and the wall of the 300 μm-thick silicon diode is only 90 μm along two of the chip edges, requiring a wedge aluminium wire bonding technique for bonding the input/output pads of the chip to the surrounding printed circuit board carrier.

Fig. 1 shows the pixel schematic. Each pixel contains an integrating input amplifier, an array of eight storage capacitors and an output amplifier. Both input and output amplifiers are implemented with a folded cascode configuration using a p-type common source input transistor (Barna *et al.*, 1995). Although this configuration has a very poor power supply rejection ratio, it is very simple to lay out since it requires only four equally sized MOS field-effect transistors (MOSFETs) connected in series. Bias voltage is set by three current mirrors controlled by externally adjustable current sources. With the reset switches closed (IR and OR for the input and output cascode amplifiers, respectively) the input and output nodes of each amplifier are forced to the same voltage, namely 3.5 V for a typical bias current of 10 μA. Current integration into the input cascode amplifier forces the output node toward the ground level. Power consumption is 100 μW per pixel.

Detector operation consists of two steps: an integration/storage sequence of up to eight full frames and a subsequent readout sequence. To start the integration period, the store enable switch (SE) is closed, the read enable switch (RE) is opened, a storage capacitor (C1–C8) is selected, and the output reset switch (OR) is closed fixing the voltage at the bottom plate of the selected storage capacitor (Fig. 1). When the reset switch (IR) is opened, the input amplifier integrates the X-ray induced current onto the integration capacitor with the resulting voltage stored across the selected storage capacitor. At the end of the frame integration, the storage capacitor is electrically isolated from the circuit with CMOS switches. After resetting the input amplifier and clearing the integration capacitor a new storage capacitor can be connected to the input amplifier for the next frame integration period. This procedure can be repeated until the on-chip analog memory of eight storage capacitors is filled. At this point the store enable switch (SE) is opened, the read enable switch (RE) is closed, and the readout sequence takes place by sequentially reading all stored capacitor voltages through the output stage of each pixel and multiplexing onto the serial output line for off-chip digitization.

The integration time is externally selectable using a logic gate pulse of duration from 1 μs up to several minutes. The practical upper limit for integration time is set by the leakage current of the pixel diode. The minimum time between two successive frames (400 ns) is limited in the present design by the time required to reset the integration capacitor in the input stage.

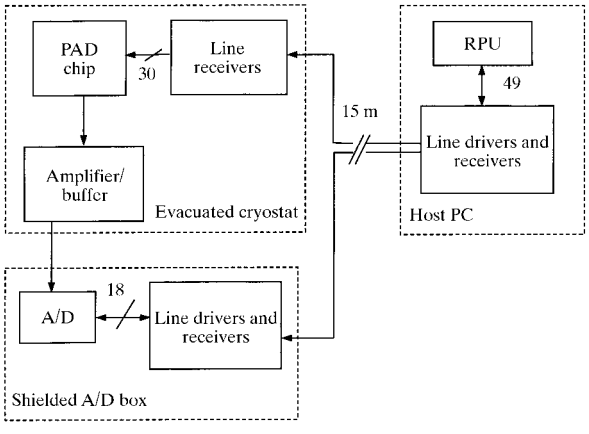

Figure 2
Schematic diagram of the logic components of the PAD system. The amplifier/buffer is an operational amplifier follower (AD845, Analog Devices, Norwood, MA, USA) with a gain of 2, which serves to scale the output voltage of the PAD chip to the input range of the analog-to-digital converter (ADC4322, Analogic Corporation, Wakefield, MA, USA). Numbers above hatch marks indicate the number of signals in the respective buses. 15 m cables separate the detector module from the host PC. Power supplies are omitted for clarity.

3. Detector controller

In Fig. 2 the three major elements of the PAD system are shown: the PAD detector, the analog-to-digital (A/D) converter unit (2 MHz 16-bit converter, model ADC4322A, Analogic Corporation, Wakefield, MA 01880, USA), and the PAD controller which is implemented with a reconfigurable processing unit (RPU) hosted into a personal computer and is used for controlling X-ray signal integration and readout of the PAD. The overall system is completed by ancillary electronics units such as voltage regulators, trimmers, differential line drivers and receivers, all mounted on custom-designed printed circuit boards. The PAD chip modules are small printed circuit boards carrying a wire-bonded chip fastened to a ceramic substrate which are connected to a mother board. This arrangement allows PADs to be changed easily during testing. The RPU is an XC6216 (Xilinx, San Jose, CA, USA), interfaced to the host PCI (peripheral component interconnect) bus on a HOT Works Development System card (Virtual Computer Corporation, Reseda, CA, USA). This chip contains a 64 × 64 array of logic units, each of which in effect is a 1-bit computer with copious uncommitted routing resources to permit software interconnections of the logic units in nearly arbitrary arrangements.

Two different modes of operations for the RPU were developed. The simplest, but most flexible, interface to the PAD was a one-to-one mapping of the signal lines to input or output registers that could be read or written, respectively, by software. In this mode the RPU used the PC clock for synchronizing its operations, but this simple approach has two drawbacks. One is that signal integration time was limited by computer speed to a minimum of 5 μs, with a 25 μs dwell between successive image frames. The second and more severe limitation is timing jitter affecting the performances of the PAD during the integration procedure. This effect was introduced by task switching of the personal computer operating system. However, this mode offered the essential features of easily writing and modifying files of control words (bit patterns) to find the optimum sequence

Table 1
Measured device characteristics for three chips.

Values given in terms of X-rays refer to equivalent numbers of 8.9 keV X-rays. One analog-to-digital converter unit (ADU) is 1/65536 of 5 V. Values are calculated on a per pixel basis and represent the average of the eight storage frames. The range of observed values for three different chips is indicated for noise and dark current. Within a given chip, pixel-to-pixel variation in the read noise was less than 15%, and variation in the dark current was less than 20%.

RMS read noise†	2.0–2.8 X-rays pixel^{-1}
Dark current (253 K)	6.2–30 fA pixel^{-1}
Dark current (253 K)†	1.6–7.7 X-rays pixel^{-1} s^{-1}
Full well capacity†	17000 X-rays
Non-linearity (% full well)	<0.2%
Quantum efficiency based on stopping power of diode layer	97%
Integration capacitance	2 pF
Conversion gain†	2.75 ADU X-ray^{-1}

† X-ray units are for 8.9 keV X-rays.

and timing of commands to the PAD, a vital step in the development of the system.

To improve performances the RPU was devised to run independently from the PC clock during the integration sequence. This was achieved by using the on-board RPU programmable clock during the integration sequence and synchronizing it to the PC clock only during the detector readout sequence and data transfer into the PC hard driver. Hence, a design was developed to implement a state machine (Horowitz & Hill, 1989) in the RPU that autonomously cycles through the states needed to acquire eight image frames (integration sequence). The RPU on-board clock was operated at 20 MHz, giving a timing resolution of 50 ns. This allowed a minimum integration time down to 150 ns, and the minimum time between frames of 800 ns, which is set by the data-acquisition clocking speed. Maximum integration time using this state machine is 214 s per frame, well beyond any testing that was attempted.

There are several advantages to this design approach. The foremost is simplicity of reconfiguration: connections of signals to the pins of the RPU were assigned arbitrarily because all wiring interconnections are made in software. Consequently, hardware construction and software design can take place concurrently. The design is also very flexible in that the same electronics can be used, not only for the PAD, but also for the many different types of test chips that are being generated in the project: only software changes are required to accommodate the differing configurations. Finally, the design can be improved over time, without necessitating hardware modifications.

4. Detector characterization

Out of a set of 95 chips fabricated, 87 were bump-bonded to a silicon diode layer while eight were bonded to a GaAs layer. The GaAs chips have yet to be fully characterized and are not discussed here. 20 of the silicon diode bump-bonded chips were wire-bonded to chip carriers. Of these, three were fully characterized at 253 K. An additional set of ten chips was tested in a more limited manner at room temperature to search for systematic problems in fabrication or the bump-bonding process. All tested chips showed more than 99% working pixels with the exception of one device which had several percent dead pixels. Based on this limited set of randomly selected devices, we conclude that the bump-bonding process was successful with acceptable yield.

A few chips showed limited imaging ability, most likely due to a fault in either a column or row address line. A second type of defect observed on a few chips consisted of a single isolated column having a considerably lower gain with respect to the others. This defect did not affect neighboring columns or compromise the imaging ability of the device. These effects may be attributed to random defects in the CMOS chip fabrication, but could also have been induced on the chip during the assembly process (*i.e.* bump-bonding, chip fastening, wire bonding). Since it was known from the start that fabrication would yield many more chips than would be used at this preliminary stage of design, little attention was given to fault-tolerant design to optimize the yield of acceptable chips. The fact that most of the chips from the first large-scale fabrication run were good suggests that eventual yields might be quite acceptable.

Fully characterized chips were cooled to 253 K within a vacuum cryostat having a light-tight X-ray transparent window. The diode layer was biased to an over-depletion voltage of 60 V. All chips run with the same clocking pattern and bias voltages were adjusted on each chip to give the same current bias in the cascode amplifiers.

A variety of input signals was used in the characterization. Imaging with visible light proved to be extremely useful for the initial set-up of bias voltages and clocking sequences. The thermally generated dark current within the diode layer provided a source of stable uniform current useful for noise characterization. The devices were also characterized with X-rays, using both a conventional laboratory generator and an intense synchrotron beam that allowed characterization of the device on the microsecond time scale. A summary of the detector parameters for the three fully tested chips is given in Table 1.

4.1. *Pixel well depth*

'Well depth' (the pixel saturation signal) was found by integrating the thermally generated dark current of the chips at 293 K. At this temperature, pixel capacitors fill within 3 s. Saturation was found to occur at a level of 44000 ADU (3.36 V or 17000 8.9 keV X-rays).

4.2. *Dark current*

Dark current at 253 K was measured for each device using a range of integration times from 25 ms to 1.4 s. These data were also used to compute the linearity and electronic noise for each pixel within a given chip. The tested detectors had dark currents ranging from a high of 0.03 pA pixel^{-1} to 0.006 pA pixel^{-1}, with the pixel-to-pixel

variation within a given chip of the order of 10%, including pixels at the edge of the diode layer. At these currents it takes more than 2000 s to saturate the integration capacity of a pixel. Note that this represents a significant improvement over earlier prototype devices within our group (4 pA pixel^{-1}; Eikenberry *et al.*, 1998). This decrease in dark current is due to both a lower operating temperature and improved processing of the diode layer. Obviously, even lower dark currents could be obtained by further cooling.

4.3. *Read noise*

The noise in an image is due both to an inherent electronic noise floor (read noise) of the amplifier chain and to the shot noise associated with the statistics of recording a given number of quanta in a pixel. The read noise floor determines the lower threshold of detectable illumination and can be computed from frames taken without illumination or appreciable dark-current accumulation. The RMS read noise was fairly consistent among the tested chips with a level of 0.5 mV (6.6 ADU), equivalent to the signal from 2.6 X-rays of energy 8.9 keV (Table 1).

4.4. *X-ray response*

The response to X-rays was measured at a variety of incident X-ray fluxes and integration times. Initial characterization was performed with a sealed-tube X-ray source (Enraf-Nonius Diffractis 601 with fine-focus Cu tube) and graphite crystal monochromator (Blake Industries, Scotch Plains, NJ, USA) set to select K_β (8.9 keV) radiation. K_β radiation was used to characterize the detector in order to closely match the energy used in the synchrotron radiation tests. Tube voltage was kept below 15 kV to eliminate higher-order harmonics passing through the monochromator. Slits were used to define a beam 0.9 mm × 0.6 mm. A flux of 14463 X-rays s^{-1} was calibrated with an NaI scintillator and photomultiplier (model 1XM.040BP, Bicron Corporation, Newbury, OH 44065, USA). Frame integration times of 1 s were used to average the 120 Hz time structure of the X-ray tube output. A conversion factor of 2.75 ADU X-ray^{-1} was found.

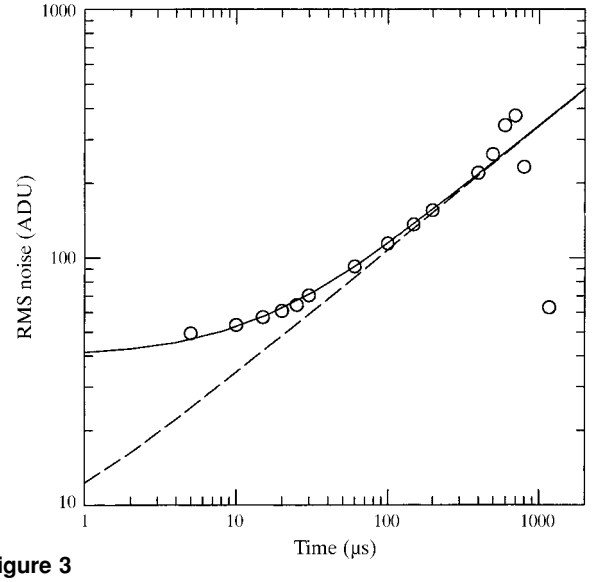

Figure 3
RMS noise per pixel *versus* integration time for an incident flux of 20 X-rays pixel^{-1} μs^{-1}. X-ray energy is 8.9 keV with a conversion gain of 2.75 ADU X-ray^{-1}. The solid line is a fit to the data using $\sigma^2 = \sigma_{\rm read}{}^2 + gN$, where σ is the measured noise, $\sigma_{\rm read}$ is an assumed fixed read noise per pixel, g is the conversion gain (ADU X-ray^{-1}) and N is the number of X-rays integrated per pixel. The fixed read noise of 40 ADU that was found is much higher than the noise of 6 ADU found with zero X-ray flux. The dashed line shows the expected noise if this lower read noise floor was realised. At times above 500 μs the pixel full well is reached, causing the measured noise to deviate from Poisson behavior.

X-ray conversion in silicon yields 2440 electron–hole pairs for an 8.9 keV photon (using 3.65 eV per electron–hole pair; Janesick *et al.*, 1988). Assuming a designed integration capacitance of 2 pF and an ADU step of 76.3 μV (65536 levels in 5 V), one would expect a conversion factor of 2.56 ADU X-ray^{-1}. This is in good agreement with the measurement, given the tolerance in the value of the integration capacitance.

4.5. *High-speed imaging of intense steady-state signals*

The characterization of the detector response to X-rays in the sub-millisecond regime was carried out with a synchrotron beam. A monochromatic beam from the D1 beamline at the Cornell High Energy Synchrotron Source (CHESS) was used to illuminate the detector surface directly. This is a hard bending-magnet beamline fitted with a 1% bandpass double-bounce multilayer monochromator. The monochromator was tuned to below the *K*-edge of copper at 8.9 keV. The incident flux on the detector was adjusted using various copper foils with thickness from 25 μm to 150 μm to attenuate the beam by factors up to 1000. By using a primary beam energy just below the *K*-edge of the attenuator, the harmonic component of the beam (∼1% with no attenuation) was reduced relative to the primary beam as more attenuation was added. This provided a convenient method of varying the flux incident per pixel without unduly hardening the beam. The beam spot size was set using slits to 15 × 2 mm^2, corresponding to the maximum deliverable beam size. This illuminated a substantial portion (6.5%) of the active area. Although not required for detector operation, a mechanical shutter was used to limit the exposure time of the detector to the intense X-ray beam to less than 100 ms per image, as radiation damage of the integrated circuit chip was a concern.

A series of frames was taken with an incident flux of ∼20–35 X-rays μs^{-1} pixel^{-1}, depending on position, and with integration times ranging from 1 to 500 μs, the latter corresponding to pixel-well saturation. At each time step, 19 exposure sets were collected where each set consisted of the images from the eight storage capacitors. A background image (an integration of dark current only) was subtracted from each exposure. The recorded dose in each image was scaled using the reading from a helium-filled ion chamber

to correct for the gradual decay in the intensity of the synchrotron beam.

From this data set the response linearity, well depth and detector noise (Fig. 3) were extracted for each pixel of the detector. The detector response had a maximum non-linearity of 0.5% between 15 and 500 μs, the time at which saturation occurred. The pixel well depth was 16580 X-ray photons (8.9 keV) with a pixel-to-pixel uniformity of better than 1% across the illuminated area. This is in excellent agreement with values measured at lower frame rates using the pixel dark-current signal (Table 1).

The noise in the X-ray images was computed as a function of X-ray dose for each pixel in the illuminated part of the image. Using a series of 19 images with the same integration time, the standard deviation of the values of a given pixel was computed. In the exposed region of the chip, the curve of noise *versus* integration time follows the expected behavior of the Poisson statistics at higher dose (Fig. 3). As the integrated dose goes to zero, we observed a significantly higher read noise floor of 40 ADU in the exposed region as compared with 6 ADU found with the measurements taken at lower flux (Table 1). The noise in the unexposed regions of the chip was much closer to that of the low flux measurements, indicating that the higher noise in the exposed region is signal induced (see below).

4.5.1. *Departures from ideal behavior*. In addition to an increased noise floor, we observed several other anomalous phenomena associated with high fluxes and short integration times. One anomaly encountered at high X-ray fluxes (>1000 X-rays μs^{-1} $pixel^{-1}$) was a flux-induced shift in the background pedestal level. This was manifested as integrated signals for short exposure times that were signifi-

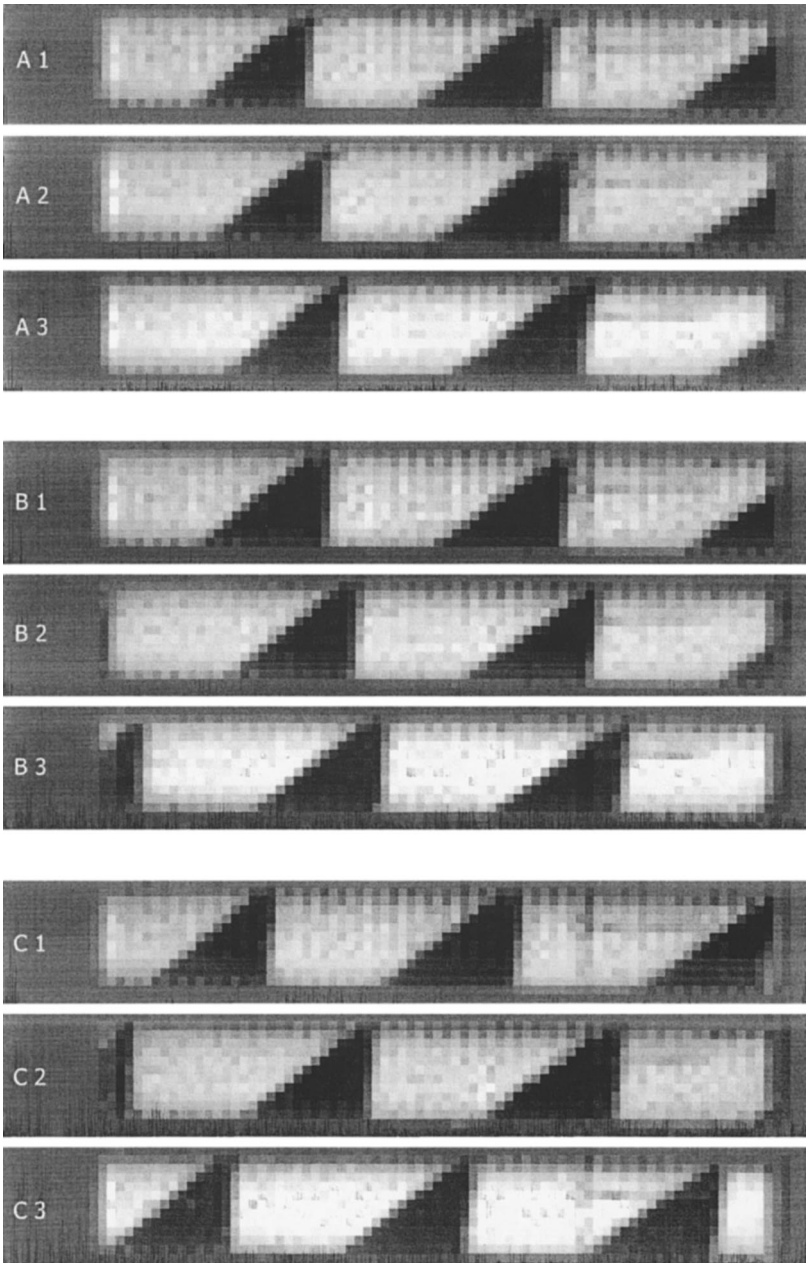

Figure 4
Time-resolved radiography of a moving saw blade. Each panel in this composite is a 14 × 91 pixel illuminated portion of a frame. Each panel shows a portion of three saw teeth (dark shadows pointing up in these images) partially occluding a 1.7 × 12 mm^2 monochromatic synchrotron beam (8.9 keV). Shown are three sets of three panels (A1–A3, B1–B3 and C1–C3), each set being the first three frames of the eight recorded in the PAD using a given integration time and interframe delay. Panels A1–A3: 5 μs integration time with 1 μs interframe delay. Exposure A2 begins 6 μs after the beginning of A1. Panels B1–B3: 5 μs integration time with 5 μs interframe delay. Panels C1–C3: 5 μs integration time with 30 μs interframe delay. Blade rotation was 5000 r.p.m. in all frames corresponding to a saw tooth speed of 48 m s^{-1}. Tooth spacing was 3 mm. X-ray flux was 2000 X-rays μs^{-1} $pixel^{-1}$. No uniformity (flat field) correction has been applied.

cantly below the nominal background pedestal value. While the linearity of response was found to be excellent, the signal extrapolated to zero integration time was significantly negative for high incident fluxes. Recall that the beam was not mechanically shuttered for each frame, but illuminated the detector continuously for 100 ms. It is likely that the intense X-ray beam induced a variation in the output cascode voltage prior to the integration period (the output cascode voltage value defines the background level), causing a transient change in the offset. Again, only those pixels exposed to X-rays showed a voltage floor different from the background. Note that the time structure of the storage ring source (4×66 ps bunches in 40 ns bunch trains separated by 294 ns) causes the instantaneous flux to be a factor of 700 higher than the average flux, or $>7 \times 10^5$ X-rays μs^{-1} pixel^{-1}. The charge collection time of the diodes ($\sim$10 ns) smooths this structure so that the CMOS sees only the 40 ns component. Even so, this induces an X-rays signal current, sunk by the cascode amplifier, that is more than 30% of the bias current, so bias shifts should not be too surprising at this level. Future designs should include either a protection circuit at the amplifier input or an input amplifier with a larger current capability.

There is also some direct conversion of X-rays within the CMOS electronics layer which may play a role in the observed anomalous behavior. Although they are primarily absorbed in the detective diode layer, some X-rays are absorbed in the CMOS electronics layer generating mobile charges. Charge generated in this manner could affect the behavior of various electronic elements for a time scale longer than a few tens of milliseconds (see below). This effect is distinct from the long-term radiation damage of the electronics discussed below, as it is seen to recover quickly. More tests and simulations need to be performed in order to identify the true nature of these anomalies.

Finally, a gain difference between odd and even pixel columns was not observed at frame rates less than 10 kHz. The source for this behavior may be attributed to the asymmetric pixel layout of the CMOS readout channel. Although the pixel elements in the diode layer are square, they are mapped to rectangular cells in the CMOS layer, which facilitates the bussing of signal lines. Future work on modeling of the parasitic elements of the CMOS chip layout will address this issue of gain asymmetry.

4.6. *High-speed imaging of time-varying signals*

Two different imaging tests were performed at the CHESS D1 beamline with the aim of probing the time-resolved capabilities of the detector. First, a fast-moving object was imaged in a radiography experiment with the monochromatic beam described above. Second, Laue diffraction was obtained from a rapidly rotating test sample placed in the white synchrotron beam.

4.6.1. *Time-resolved radiography.* To test the rapid imaging capabilities of the device, the teeth of a high-speed circular saw were imaged directly using X-ray absorption. A portable circular saw (Black & Decker) with a 184 mm-diameter fine-toothed plywood blade was mounted such that the blade was 30 mm in front of the detector. The saw blade had 140 teeth, each 2.5 mm high and 3 mm wide. The monochromatic (8.9 keV) beam (described above) was defined to be 1.7×12 mm^2. This was used to image a portion of three adjacent teeth on the blade. Blade speed was adjusted by varying the AC voltage applied to the saw with a variable transformer. Rotation speed was monitored by a LED/phototransistor assembly. Maximum rotation speed was 5000 r.p.m. corresponding to a linear speed for the saw teeth of 48 m s^{-1} (0.3 pixels μs^{-1}).

Fig. 4 shows three sets of images taken of the blade rotating at maximum speed. Each set is a composite showing the first three frames of the eight recorded. Each data set has a frame integration time of 5 µs. The inter-frame delay was varied between the sets, with the data shown corresponding to 1, 5 and 30 µs delays, respectively. The expected 0.3 pixels μs^{-1} displacement is observed. Some smearing due to the blade movement during the integration time can also be observed. The average flux on the illuminated area was 2000 X-rays μs^{-1} pixel^{-1}.

The area in each image that is shadowed by the saw teeth was negative in the background-subtracted image, indicating a downward bias level shift in the irradiated part of the image. In images taken of a static saw blade, these shadowed regions were not negative but at the background bias level. As noted above, regions exposed to high flux showed anomalous behavior, probably due to shifts in the output voltage of the cascode amplifier. The behavior seen in the moving images is again a manifestation of the same anomaly. The observed negative values in the moving blade images suggest there is a memory for this behavior with an associated time constant. By slowing the blade speed to zero, one should return the shadowed areas to a non-negative reading. Measurements taken with blade speeds as low as 64 r.p.m. showed no difference in the shadowed regions as compared with the fastest rotation. This corresponds to areas being blanked for up to 6 ms, indicating the time constant to relax is much longer than this. We also observed that laser illumination of the PAD (which is light sensitive), which fills the pixel well within a few microseconds, does not produce the bias level shift effect. This leads us to believe that the bias level shift may arise from X-ray conversion in the CMOS components of the detector.

4.6.2. *Transmission Laue diffraction of moving polycrystalline samples.* The time-resolved Laue diffraction tests were performed on the CHESS D1 bending-magnet beamline, which was set up in white-beam (polychromatic) mode by removing the multilayer monochromator from the beam path. Unfortunately the detector used for this experiment was the unit which had several percent bad pixels. Although a better device might have been selected, the essential features can still be seen. The sample in this case was a 180 mm-diameter 1.5 mm-thick disk of type 3003 bendable aluminium sheet. This specific aluminium was selected for its large grain size (0.1–0.5 mm) which

produced an intense diffraction pattern featuring radial streaked lobes of diffracted intensity (Fig. 5). The disk was mounted on a circular saw with a rotation rate of 2500 r.p.m. The beam size was set to 1×1 mm^2 and the sample-to-detector distance was 30 mm. For this experiment an integration time of 100 µs with frame delay time of 25 µs was employed yielding 8 images ms^{-1}.

Each grain from the polycrystalline aluminium sample formed its own Laue pattern over the energy range 5–25 keV. The strong peaks visible in the images are the superposition of many highly oriented grains of the sample. The eight images were obtained as the disk rotated through an angular range of 15°. About 13000 X-rays pixel^{-1} were recorded in the brightest diffraction peaks corresponding to 80% filling of the pixel well. Transmission Laue patterns on an Al–Li 2090 aluminium alloy (Haase *et al.*, 1998; Strock *et al.*, 1995) also shows similar radial streaks and has been used with X-ray microbeams to map the fatigue cracks that develop under too much stress.

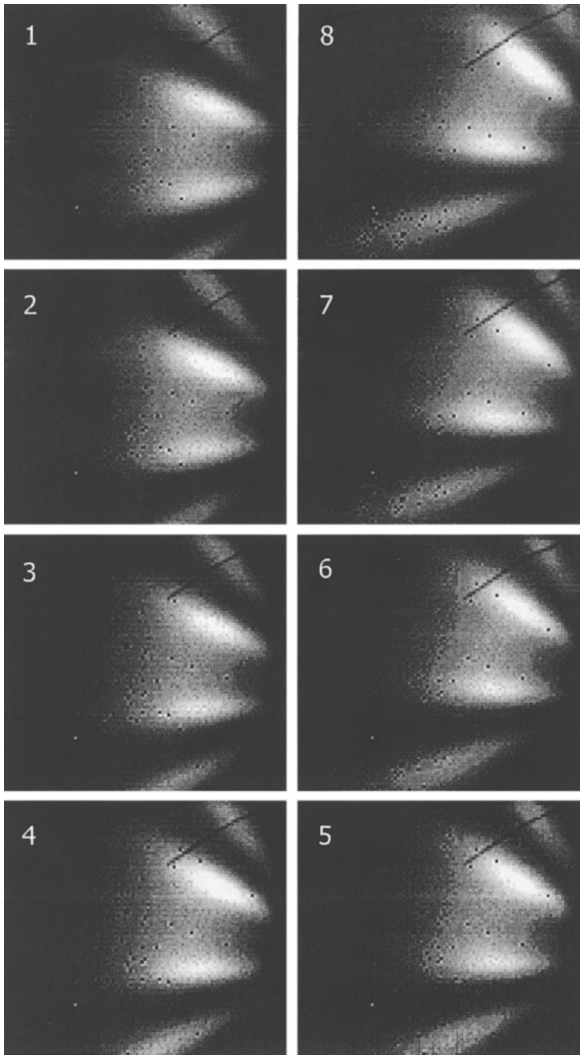

Figure 5
Laue diffraction from a polycrystalline aluminium disk rotating at 2500 r.p.m. A beam of size 1×1 mm^2 impinged upon the 180 mm-diameter disk ~10 mm from its periphery. Sample-to-detector distance was 30 mm. The peaks visible in the images are the superposition of many oriented grains of the sample. The eight images were obtained as the disk rotated through an angular range of 15°. Integration time was 100 µs per frame with 25 µs interframe delay. Frames are labeled in sequence from 1 to 8. Image 8 is placed next to image 1 to highlight the angular change in the diffraction pattern. The beam position was off the imaging area to the right of each frame. In the upper right of each image one can see the shadow of the 100 µm-diameter wire used to bias the front surface of the diode layer.

4.7. *Radiation damage*

Conventional CMOS-FET technologies featuring minimum gate lengths longer than 1 µm are extremely sensitive to damage induced by ionizing radiation. In the case of CMOS integrated circuits, X-ray absorption in both field and gate oxide induces variations of transistor parameters, such as threshold voltage and leakage current, that causes devices to cease functioning with a deposited dose as low as 30–60 krad (SiO_2) (Johnston, 1998; Osborn *et al.*, 1998). For synchrotron radiation applications, particularly for time-resolved diffraction measurements in the microsecond range, a similar total dose could easily be delivered to the CMOS readout electronics during a period of a few minutes to a few hours, thereby inducing a drastic premature aging of the device.

To quantify the radiation-damage sensitivity of the PAD electronics, we irradiated the chip with a monochromatic

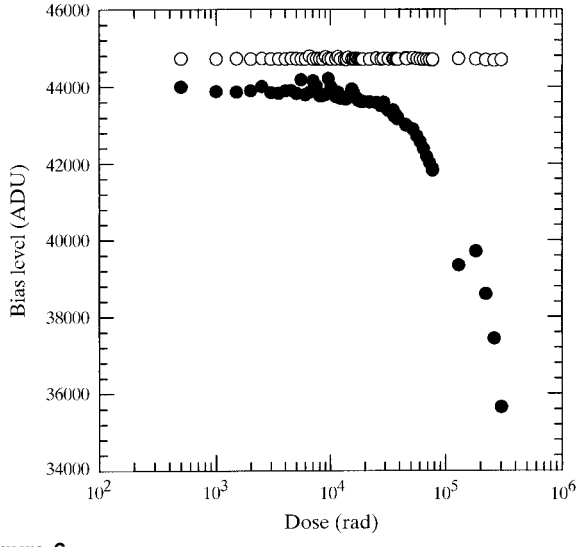

Figure 6
Change in output bias level of the cascode amplifier for increasing radiation dose to the silicon oxide (SiO_2) layer in the CMOS pixel electronics. A region of the chip was irradiated with 8.9 keV X-rays at a rate of 1–3 krad (SiO_2) s^{-1} in sequential 100 ms periods. Background exposures were taken after each 100 ms radiation dose to monitor bias level shifts. The filled symbols show the bias level for an exposed region as a function of total accumulated dose. Clear effects can be seen after 30 krad. The open symbols show the bias level from an unexposed region in the same device (vertically offset by 1000 ADU for clarity).

beam of 8.9 keV X-rays as in the above tests with an estimated dose rate of 1–3 krad (SiO_2) s^{-1}. Note that this is the dose at the CMOS oxide layer after the beam has been attenuated by the diode layer. A portion of the chip, about 700 pixels, was directly exposed to the synchrotron beam. A computer-controlled mechanical shutter controlled the dose. Each detector exposure lasted 70–100 ms during which time the X-ray signal was integrated for 10 μs. A background image with no X-ray illumination was collected after each exposure. This procedure allowed the study of progressive damage induced by X-ray irradiation with no annealing time.

By monitoring the pedestal level in the series of background images one can clearly see the effects of radiation damage. Fig. 6 shows that by 30 krad (SiO_2) a significant shift in pedestal value has occurred within the exposed regions. The unexposed regions continue to exhibit normal behavior. This test is very sensitive since it is directly dependent upon the transistor voltage threshold values. Inspection of the X-ray images showed that, again, the principal damaging effect was a shift of the cascode bias point. The switching functionality of the detector remained unaffected as all eight frames were accumulated. Note that proper images can still be obtained by subtracting a contemporaneous background, which will have the same radiation-induced offset. However, this offset reduces the full-well capacity of the pixel, so that imaging eventually becomes impossible.

The radiation hardness of the prototype detector is clearly a concern as the current radiation tolerance of the CMOS layer [less than 100 krad (SiO_2)] is not suited for high photon flux applications. However, the high-energy physics community at CERN (Faccio *et al.*, 1998) has recently shown that radiation hardness of a CMOS transistor is intrinsically high in the deep-submicron technologies (minimum feature size <0.25 μm) now available through commercial vendors. Here the gate oxide thickness is less than 10 nm. When used in conjunction with an appropriate layout technique, negligible damage in a pixellated detector is observed with total doses as high as 30 Mrad (Campbell *et al.*, 1998). This layout technique employs closed-gate transistors and guard rings to prevent leakage paths between the source–drain contacts of MOS transistors and among adjacent devices. We are already designing test chips with a 0.5 μm Hewlett-Packard submicron technology since their 1.2 μm process used in this study will be soon phased out. We plan to investigate the radiation tolerance of this process as well as that of a 0.25 μm process.

There has been relatively little attention given to transient effects resulting from X-ray conversion and consequent charge deposition in the CMOS. As mentioned earlier, this may be responsible for the bias shifts described in §4.4. For a given X-ray flux and X-ray energy, these effects can be simulated if the carrier lifetimes and field distributions are known. The same design changes that enhance radiation tolerance may also serve to reduce transient charging. Evaluation of these effects is an important area for future investigation.

5. Conclusions

We have built and tested a prototype 100 × 92 pixel PAD. The detector was scaled up from a previous 4 × 4 pixel device and incorporated improvements to both the diode layer and the solder bump process. Although this is only one in a series of test chips leading toward a final pixel array, the detector demonstrated imaging capability with microsecond time resolution and a wide dynamic range with both monochromatic and white-beam conditions. The tests have identified aspects that need to be improved in the next round of fabrication, namely the need for better power distribution on the chip, better and faster amplifiers, and a higher-speed readout structure.

The RPU-based PAD controller gave excellent performance for the present single-module PAD. However, larger arrays of chips will require a different organization to enable more extensive multiplexing of analog and data channels. The larger RPUs that are now available should easily be able to handle the additional complexity.

Future CMOS fabrication at a smaller feature size offers a number of potential advantages. As mentioned above, deep sub-micron processes have been demonstrated to be radiation hard. The smaller features also allow for more complex electronics to fit within the pixel area as well. The next round of test PADs will also incorporate single-stage operational transconductance amplifiers with differential input for the input and output amplifiers, rather than the cascode amplifiers used in this generation of devices.

To be useful in a wider variety of X-ray diffraction applications the detector must cover a larger area, with a format of at least 1000 × 1000 pixels. The size of CMOS devices fabricated with available commercial processes appears to be limited to the 15 × 15 mm^2 format used in this work. This is limited by the step-repeat size set by the masks and imaging optics on the fabrication line. To increase the size of the active area we are contemplating several tiling schemes. One obvious solution is to tile many independent small devices into a larger array. This poses some problems with dead areas and intermodule alignment. Another option, with less dead area, is to use a larger detective diode array to accept many CMOS modules. Signal and power distribution to the CMOS could be accomplished using additional metallization layers on the diode layer itself.

We gratefully acknowledge the help of Dennis Brown, ESEC Industrie, Phoenix, Arizona, and Roland Heitmann, ESEC Industrie, Selzach, Switzerland, for their support on gold wire bonding of the first CMOS chip samples; Jack Place, Physics Department (LNS), Cornell University, for his essential work of wedge bonding the many CMOS chips used for this study; and Steve Casselman, Virtual Computer

Corporation, Reseda, CA, for providing useful hints and suggestions on the VCC Board Development Kit. We would like to thank Martin Novak, Cornell University, Physics Department, for his support during preparation of the beamline set-up. This work was supported by DOE grants DE-FG-0297ER14805 and DE-FG-0297ER62443 and CHESS, which is a national NSF-supported facility under grant NSF-DMR 97-13424.

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